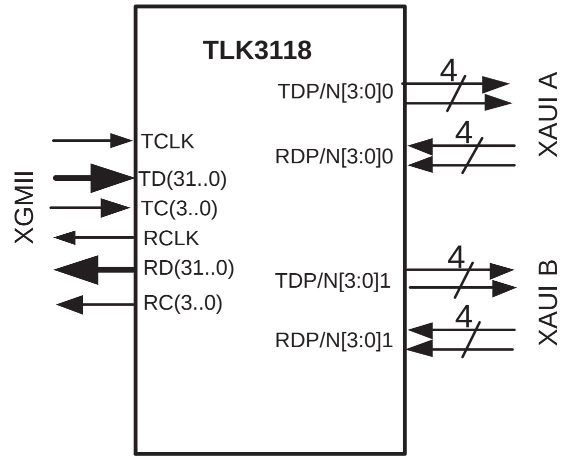
FEATURES

- Redundant Quad 3.2-Gbps Transceiver Configurable as 10-Gbps Attachment Unit Interface (XAUI) Transceiver
- IEEE P802.3ae-2002 10 Gbps Ethernet XGXS (XGMII Extender Sublayer) Compliant
- Redundancy: Fast Switching from Primary to Secondary XAUI channel with Provisionable Error Character or Local Code Fault Insertion at Switch Time
- XAUI: Transmit Pre-Emphasis and Receive Adaptive Equalization to Allow Extended Backplane Reach
- Selectable Full Duplex XAUI Retimer Mode
- Support PRBS 2^7–1 and 2^{23}– 1 Generate/verify. Support Standard Defined CJPAT, CRPAT, High Freq, Low Freq, and Mixed Freq testing
- XGMII: HSTL Class 1 I/O with On-Chip 50-Ω Termination on Inputs/Outputs
- XGMII: Source Centered Timing
- Supports Jumbo Packet (9600 byte maximum) Operation
- Align Character Skew Support of 40 bit times at Chip Pins
- MDIO: IEEE 802.3ae Clause 45 Compliant Management Data Input/Output Interface
- 1.2-V Core Voltage Supply, 1.5-V HSTL I/O Supply, and 2.5-V LVCMOS and Bias Supply
- JTAG: IEEE 1149.1 Test Interface
- Fabricated in Advanced 130-nm CMOS Technology
- Package: Small Footprint 21x21mm, 400-Ball, Fine Pitch (1mm) PBGA



DESCRIPTION

The TLK3118 is a flexible, redundant XAUI serial transceiver that is compliant to 10-Gbps Ethernet XAUI specification. The TLK3118 provides high-speed bi-directional point-to-point data transmissions with up to 12.5 Gbps of raw data transmission capacity. The primary application of this device for use in backplanes and front panel connections requiring redundant 10Gbps connections over controlled impedance media of approximately 50 Ω. The transmission media can be printed circuit board (PCB) traces, copper cables or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling into the lines.

The TLK3118 performs the parallel-to-serial, serial-to-parallel conversion, and clock extraction functions for a physical layer interface. The TLK3118 provides two complete XGXS/PCS functions defined in Clause 47/48 of the IEEE P802.3ae 10Gbps Ethernet standard. The serial transmitter is implemented using differential Current Mode Logic (CML) with integrated termination resistors.

The TLK3118 can be configured as a redundant XAUI transceiver or a full duplex XAUI re-timer. TLK3118 supports a 32-bit data path, 4-bit control, 10 Gigabit Media Independent Interface (XGMII) to the protocol device. Figure 1 shows an example system block diagram for TLK3118 used to provide the 10-Gbps Ethernet Physical Coding Sublayer to Coarse Wave-length Division Multiplexed optical transceiver or parallel optics.

DESCRIPTION CONTINUED

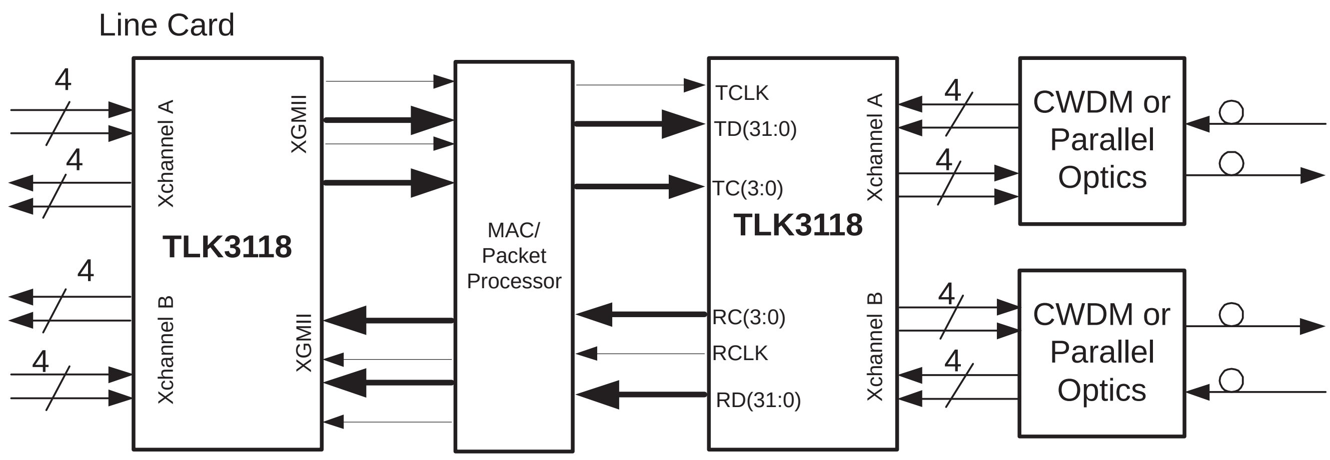


Figure 1. System Block Diagram – PCS

Figure 2 shows an example system block diagram for TLK3118 used to provide the system backplane interconnect.

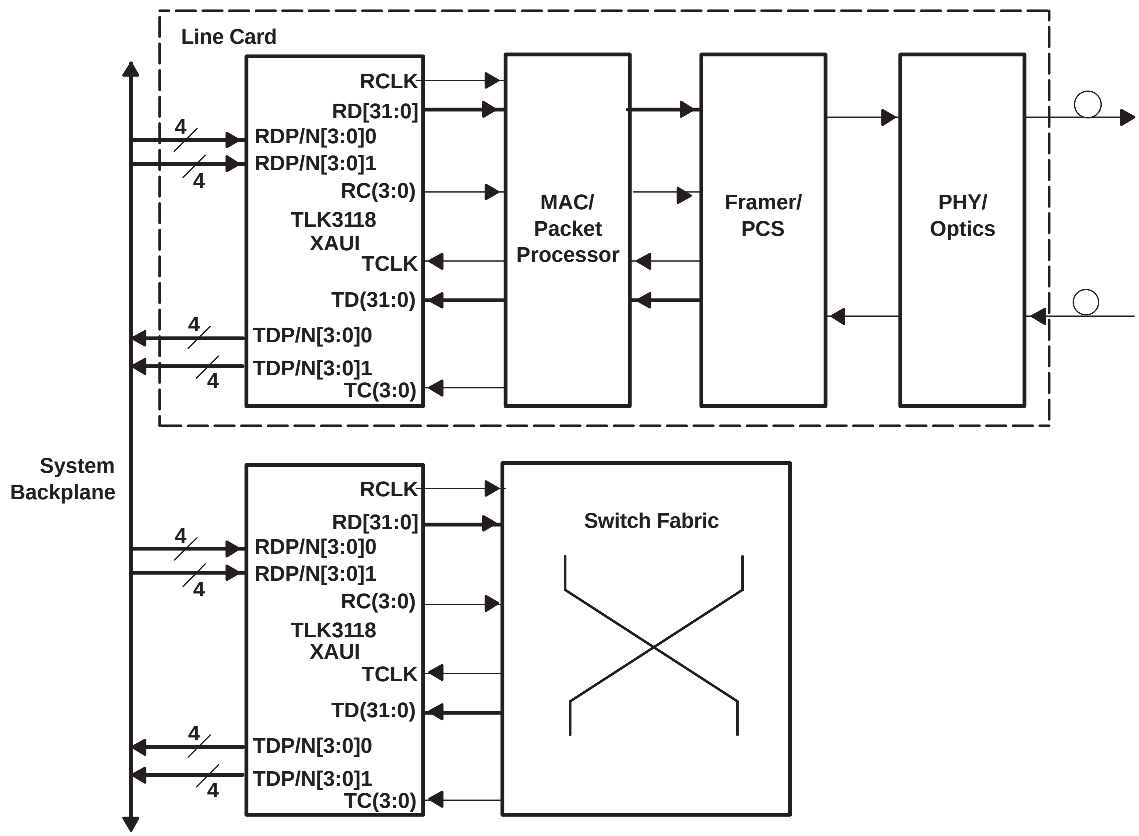


Figure 2. System Block Diagram – XAUI Backplane

The TLK3118 supports the IEEE 802.3 defined Management Data Input/Output (MDIO) Interface to allow ease in configuration and status monitoring of the link. The bi-directional data pin (MDIO) should be externally pulled up to 2.5 V.

The TLK3118 supports the IEEE 1149.1 defined JTAG test port for ease in board manufacturing test. It also supports a comprehensive series of built-in tests for self-test purposes including PRBS generation and verification, CRPAT, CJPAT, Mixed/High/Low Frequency testing.

The TLK3118 operates with a 1.2-V core voltage supply, a 1.5-V HSTL I/O voltage supply and a 2.5-V bias supply. The device consumes 1.75 watts.

The TLK3118 is packaged in a 21x21mm, 400-ball, 1-mm ball pitch Flip Chip Ball Grid Array (FC-BGA) package and is characterized for operation from 0°C to 70°C, 105°C Junction, and 5% power supply variation unless noted otherwise.

Figure 3 provides a high level description of the TLK3118.

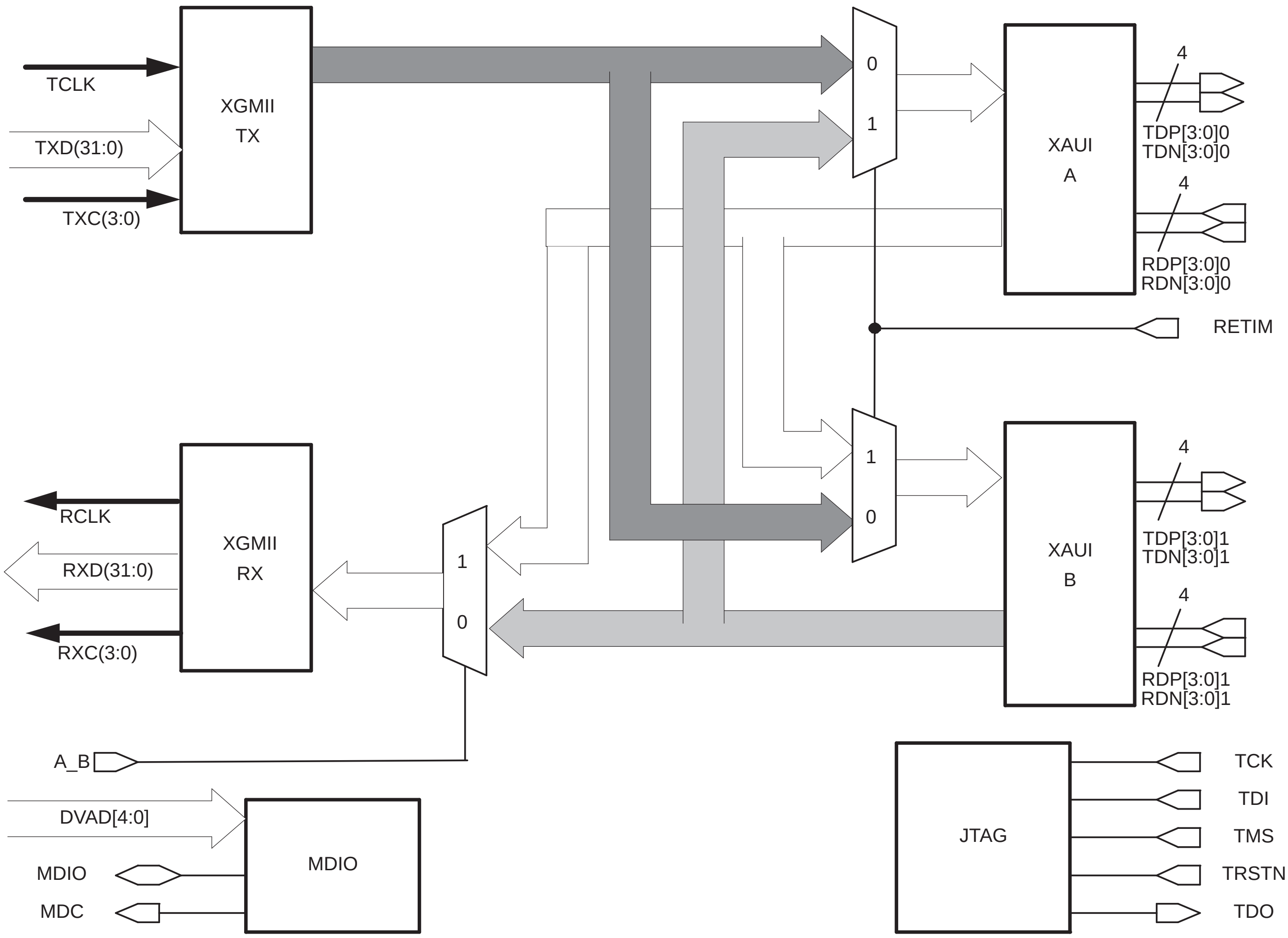


Figure 3. TLK3118 Block Diagram

Figure 4 is a more detailed block diagram description of XAUI core.

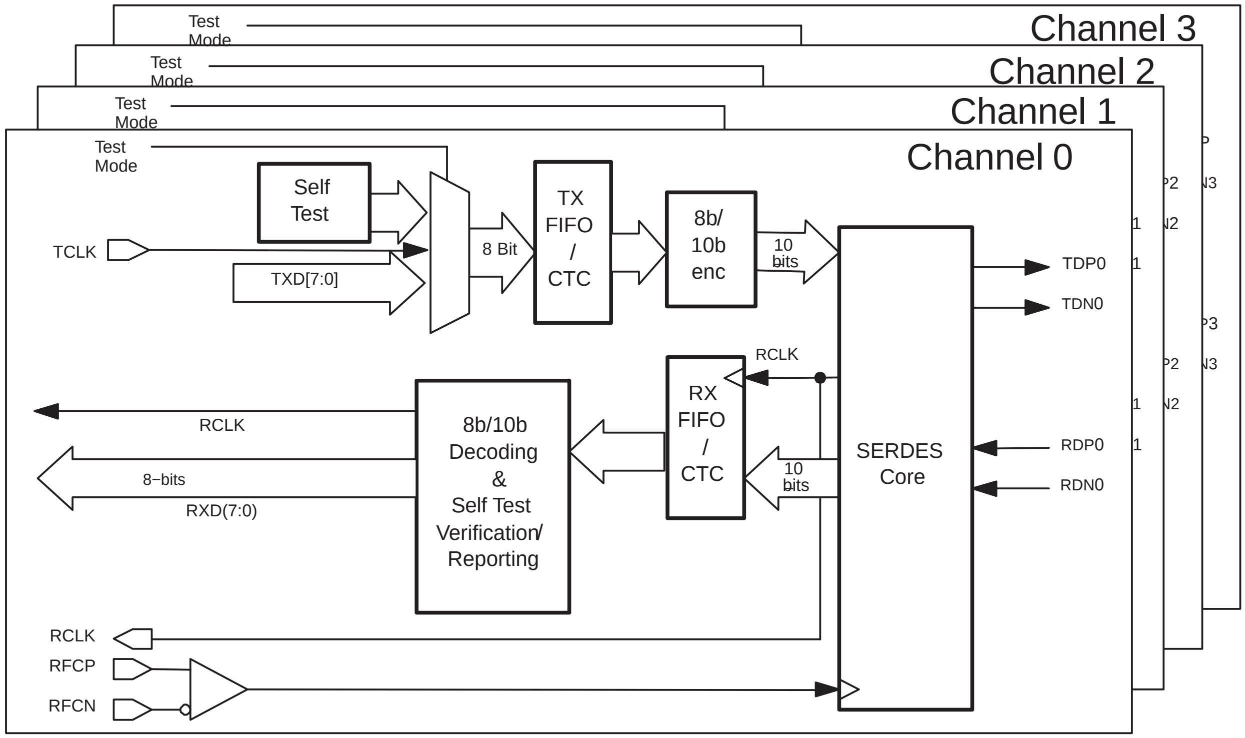


Figure 4. Detailed XAUI Core Block Diagram

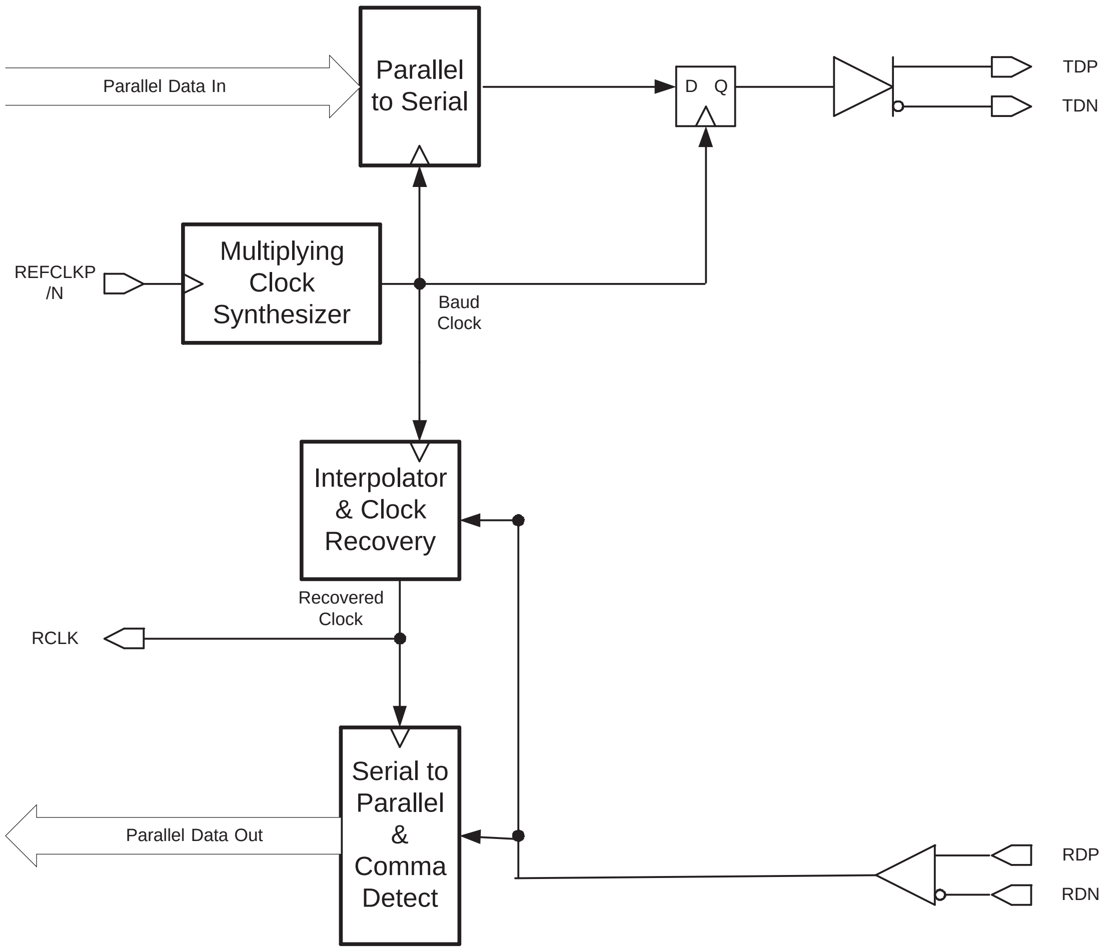


Figure 5. Block Diagram of SERDES Core

Detailed Description

The TLK3118 has two operational interface modes controlled by the state of pins A/B and RETIM. The RETIM pin controls whether the TLK3118 operates as a re-timer and the A/B pin controls which is the active bi-directional XAUI channel reflected on the bi-directional XGMII interface during transceiver mode operations.

Transceiver Operation (RETIM = LOW)

When RETIM is held low, the TLK3118 operates as a redundant XAUI transceiver. The device will serialize data input on TXD (31:0) and output on the selected serial output signals. Serial data input on selected channel is de-serialized, aligned and output on RXD (31:0) outputs. When A/B is asserted high, serial links RD [P/N] [3/2/1/0]0 form the primary XAUI channel. Data input on TXD (31:0) is output on TD [P/N] [3/2/1/0]0 and serial data input from RD [P/N] [3/2/1/0]0 is de-serialized, aligned and output on the RXD (31:0) outputs. When A/B is asserted low, serial links RD [P/N] [3/2/1/0]1 form the primary XAUI channel. Data input on TXD(31:0) is serialized and output on TD[P/N][3/2/1/0]1 and serial data input from the RD[P/N][3:0]1 is de-serialized, aligned and output on the RXD(31:0) outputs.

While communication is occurring on the primary XAUI channel, the secondary XAUI channel is fully functional capable of transmitting and receiving data. All registers are valid and accessible. The only difference between the primary and secondary channels is the primary channel is routed to the XGMII bus. The TLK3118 transceiver mode default condition will be to broadcast the data input on the XGMII inputs, TXD (31:0), to both the primary and secondary XAUI channels. The receive path of the secondary XAUI channel will default to an active state recovering and aligning data.

Detailed Description (continued)

A completely active secondary XAUI channel will allow transition from primary to secondary channels within a few XGMII clock cycles. During the transition from primary to secondary XAUI channels, the data on each byte of the XGMII bus will be 0xFE (code violation), which is the ERROR indication, or local fault indication (based on provisioned register value).

Also, when the primary input IDLE = HIGH, the secondary transmit XAUI channel transmits legal A/K/R characters instead of the 8B/10B encoded packet stream. When IDLE = LOW, the transmit packet stream is bridged to both sets of XAUI output channels.

Re-Timer Operation (RETIM = HIGH)

When RETIM is asserted high, the TLK3118 will operate as a full duplex XAUI re-timer. All the functions of transceiver operations are performed with the exception input from the XGMII. The recovered data on each XAUI channel is de-serialized, de-skewed, aligned to the reference clock, and re-serialized. In the re-timer mode inputs from the TXD (31:0) are ignored.

Note that when RETIM is high, the XAUI A receive data is eventually routed out to the XAUI B transmit serial lines. Similarly, the XAUI B receive data is eventually routed out to the XAUI A transmit serial lines.

The TLK3118 re-timer mode default condition will be to enable the XGMII receive output bus, RXD (31:0). However, a software setting is available to put the RXD bus into a high-impedance state desired for power savings. The TLK3118 can be configured, via MDIO or pin, to monitor the recovered data on either XAUI channel. If the re-timer monitoring mode is enabled, the state of the A/B pin will determine which XAUI channel recovered data is output on the XGMII receive output bus. If A/B is toggled when in re-timer monitor mode, the data on each byte of the XGMII receive output bus will be 0xFE (code violation) for several XGMII clock cycles, or local fault (based on the provisioned register value).

Parallel Interface Clocking

The TLK3118 supports source centered timing on the XGMII transmit input bus. The timing supported is the timing defined in P802.3ae Clause 46 with the TCLK centered within the transmit data bit timing, as shown in Figure 6.

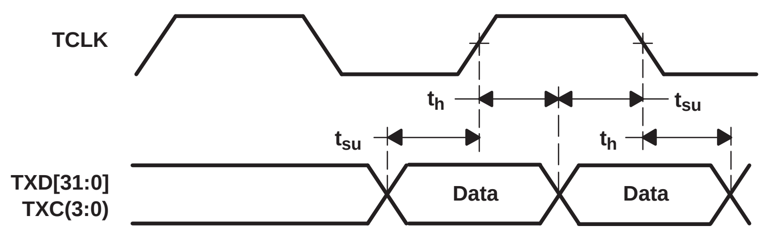


Figure 6. Transmit Interface Timing – Source Centered

On the receive data path, the data is synchronized and output referenced to RCLK, with the RCLK placed in the center of the data window, as shown in Figure 7. RCLK is derived from the transmit reference clock. A FIFO, placed on the output of the serial to parallel conversion logic for each serial link, compensates for channel skew, clock phase and frequency tolerance differences between the recovered clocks for each serial links and the receive output clock, RCLK. This FIFO has a total depth of nine ten bit entries, giving 40 bit time deskew (channel-to-channel skew) alignment capability. See Table 94 and Table 95 for more details on XGMII timing.

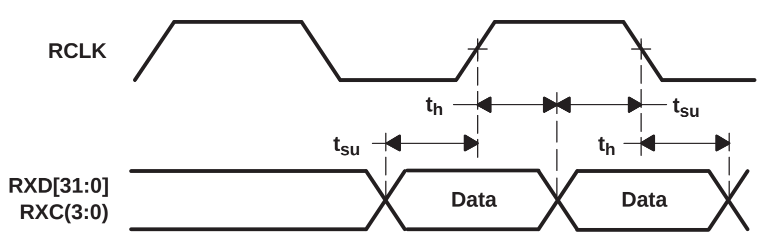


Figure 7. Receive Interface Timing

Detailed Description (continued)

Parallel Interface Data

Data placed on the XGMII transmit input bus is latched on the rising and falling edge of the transmit data clock, TCLK, as shown in Figure 6. The latched data is then phase aligned to the internal version of the transmit reference clock, 8b/10b encoded, serialized, then transmitted sequentially beginning with the LSB of the encoded data byte over the differential high speed serial transmit pins.

The XGMII receive data bus outputs four bytes on RXD (31:0). Control character (K-characters) reporting for each byte is done by asserting the corresponding control pin, RXC (3:0). When RXC is asserted, the 8 bits of data corresponding to the control pin is to be interpreted as a K-character. If an error is uncovered in decoding the data, the control pin is asserted and 0xFE is output for the corresponding byte.

Transmission Latency

For each channel, the data transmission latency of the TLK3118 is defined as the delay from the rising or falling edge of the selected transmit clock when valid data is on the transmit data pins to the serial transmission of bit 0, as shown in the following figure. The maximum transmit latency (TLATENCY) is 600 bit times; the standard allows a combined latency (TX + RX) of 2048 bit times.

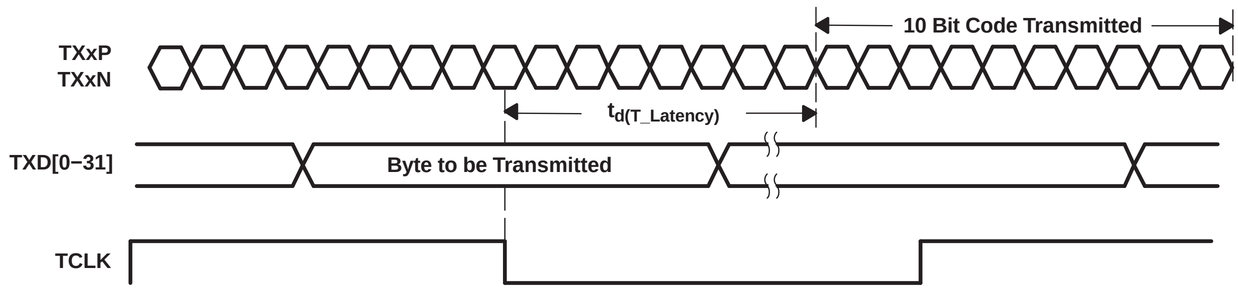


Figure 8. Transmission Latency

Channel Clock to Serial Transmit Clock Synchronization

The TLK3118 allows ±200 ppm difference between the serdes transmit reference on the XAUI side, versus the input TCLK on the XGMII side. There exists a FIFO capable of CTC operations, and has a depth of 32 locations (32 bits wide per location).

The reference clock and the transmit data clock(s) may be from a common source, but the design allows for up to +/- 200 ppm of frequency difference should the application require it.

Data Reception Latency

For each serial link, the serial-to-parallel data latency is the time from when the first bit arrives at the serial receiver input until it is output in the aligned parallel word on the XGMII, as shown in Figure 9. The maximum receive latency (RLATENCY) is 700 bit times; the standard allows a combined latency (TX + RX) of 2048 bit times.

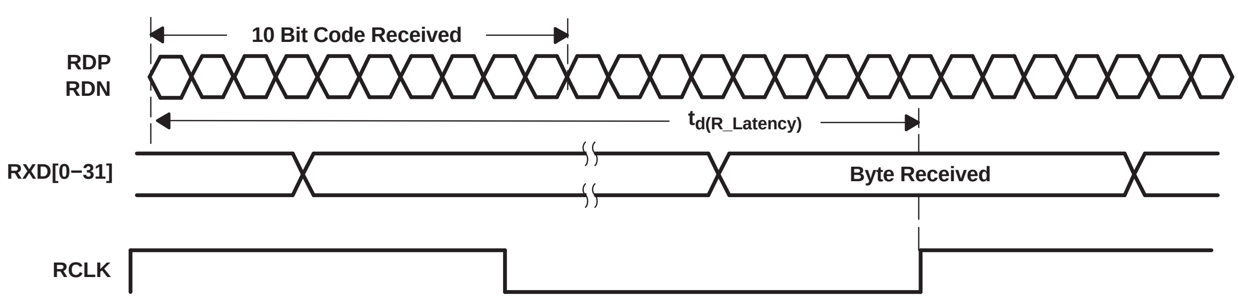


Figure 9. Receiver Latency

Detailed Description (continued)

8B/10B Encoder

All true serial interfaces require a method of encoding to insure sufficient transition density for the receiving PLL to acquire and maintain lock. The encoding scheme also maintains the signal DC balance by keeping the number of ones and zeros are balanced which allows for AC coupled data transmission. The TLK3118 uses the 8B/10B encoding algorithm that is used by 10Gbps and 1Gbps Ethernet and Fiber Channel standards. This provides good transition density for clock recovery and improves error checking. The 8B/10B encoder/decoder function is enabled for all serial links. The TLK3118 will internally encode and decode the data such that the user reads and writes actual 8-bit data on each channel.

The 8B/10B encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transition density. This transmission code includes D Characters, used for transmitting data, and K Characters, used for transmitting protocol information. Each K or D character code word can also have both a positive and a negative disparity version. The disparity of a code word is selected by the encoder to balance the running disparity of the serialized data stream.

The generation of K-characters to be transmitted on each channel is controlled by transmit control pins, TXC(3:0). When the control pin is asserted along with the 8 bits of data, an 8B/10B K-character is transmitted. Similarly, reception of K-characters is reported by the receive control pins, RXC(3:0). When receive control pin is asserted, the corresponding byte on the receive data bus should be interpreted as a K-character. The TLK3118 will transmit and receive all of the twelve valid K-characters as defined below.

Table 1. Valid K-Codes

K-Code	TXC(3:0) or RXC(3:0)	Data Bus Bytes (RXD[x: x-7] or TXD[x: x-7])	Encoded K-code		K-Code Description
			Negative Running Disparity	Positive Running Disparity	
00 through FF	0	DDD DDDDD	dddddd dddd	dddddd dddd	Normal data
K28.0	1	000 11100	001111 0100	110000 1011	IdleO/busy
K28.1	1	001 11100	001111 1001	110000 0110	IdleE/busy
K28.2	1	010 11100	001111 0101	110000 1010	
K28.3	1	011 11100	001111 0011	110000 1100	Channel Alignment Pre-Cursor
K28.4	1	100 11100	001111 0010	110000 1101	
K28.5	1	101 11100	001111 1010	110000 0101	IdleE/not-busy
K28.6	1	110 11100	001111 0110	110000 1001	
K28.7	1	111 11100	001111 1000	110000 0111	Code Violation or Parity Error
K23.7	1	111 10111	111010 1000	000101 0111	IdleO/not-busy
K27.7	1	111 11011	110110 1000	001001 0111	SOP(S)
K29.7	1	111 11101	101110 1000	010001 0111	EOP(T)
K30.7	1	111 11110	011110 1000	100001 0111	

Table 2 provides additional transmit data control coding and descriptions that have been incorporated into 10 Gigabits per second Ethernet. Data patterns put on XGMII transmit data bus other than those defined in Table 2 when the transmit control pin is asserted will result in an invalid K-character being transmitted which will result in a code error at the receiver.

Table 2. Valid XGMII Channel Encodings

Data Bus (TXD[x: x-7] or RXD[x: x-7])	TXC(3:0) or RXC(3:0)	Description
00 through FF	0	Normal Data Transmission
00 through 06	1	Reserved
07	1	Idle
08 through 9B	1	Reserved
9C	1	Sequence (only valid in Channel A)
9D through FA	1	Reserved

Table 2. Valid XGMII Channel Encodings (continued)

Data Bus (TXD[x: x-7] or RXD[x: x-7])	TXC(3:0) or RXC(3:0)	Description
FB	1	Start (only valid in Channel A)
FC	1	Reserved
FD	1	Terminate
FE	1	Transmit error propagation
FF	1	Reserved

Comma Detect and 8B/10B Decoding

When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to be able to recognize the byte boundary again. Generally this is accomplished through the use of a synchronization pattern. This is a unique a pattern of 1's and 0's that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8B/10B encoding contains a character called the comma (b'0011111' or b'1100000') which is used by the comma detect circuit to align the received serial data back to its original byte boundary. The decoder detects the K28.5 comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It then converts the data back into 8-bit data. It is important to note that the comma can be either a (b'0011111') or the inverse (b'1100000') depending on the running disparity. The TLK3118 decoder will detect both patterns.

The reception of K-characters is reported by the assertion of receive control pin, RXC (3:0) for the corresponding byte on the XGMII receive bus. When a code word error or running disparity error is detected in the decoded data received on a serial link, the receive control pin is asserted and a 0xFE is placed on the receive data bus for that channel, as shown in Table 3.

Table 3. Receive Data Controls

Event	Receive Data Bus RXD[x: 7-x]	RXC(3:0)
Normal Data	XX	0
Normal K-character	Valid K-code	1
Code word error or running disparity error	FE	1

Channel Initialization and Synchronization

The TLK3118 has a synchronization state machine which is responsible for handling link initialization and synchronization for each channel. The initialization and synchronization state diagram is provided in Figure 10. The status of any channel can be monitored by reading MDIO register 4:5.24.3:0.

Channel State Descriptions

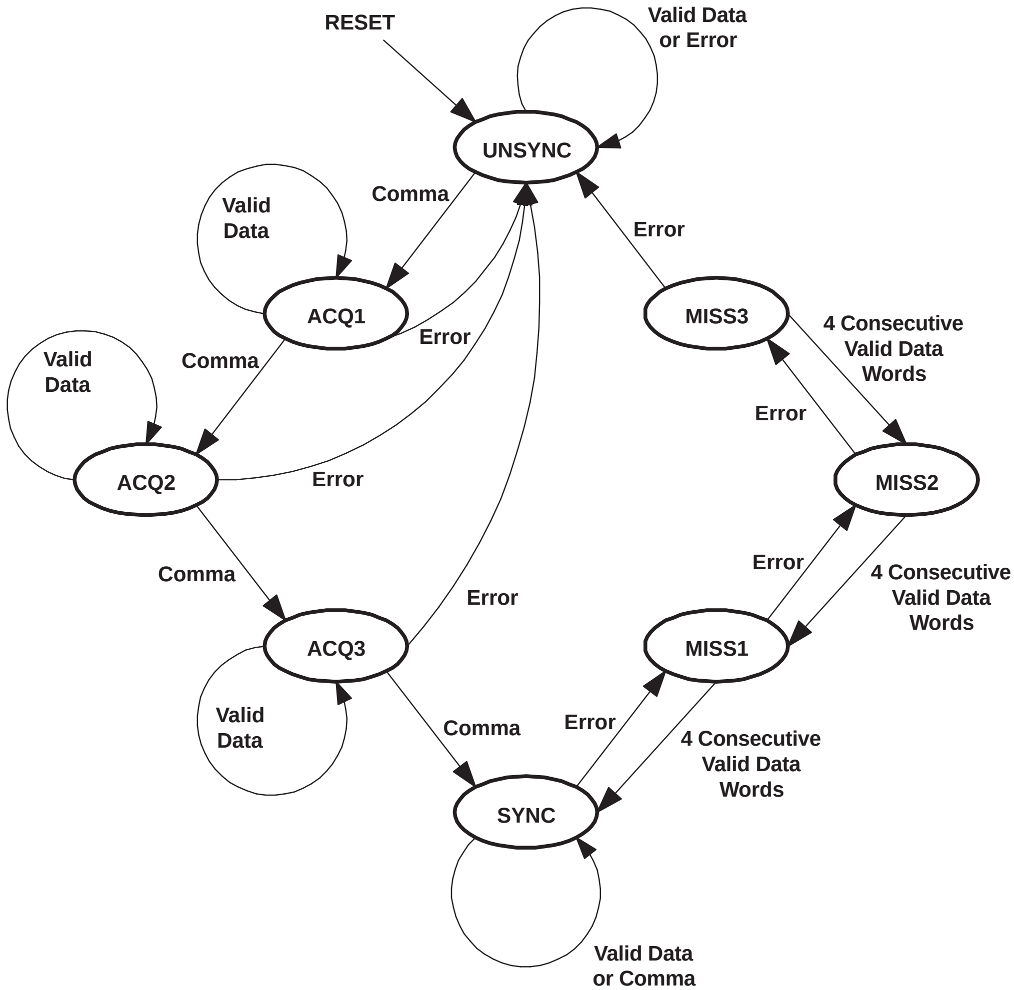


Figure 10. Channel Synchronization State Machine

UNSYNC

This is the initial state for each channel upon device power up or reset. In this state, the TLK3118 will have the comma detect circuit active and will make code word alignment adjustments based on the position of a comma in the incoming data stream. While in this state the TLK3118 will set the Lane Sync bit to '0' for the particular channel in MDIO register bits 4:5.24.3:0, indicating the lane is not synchronized. The channel state will transition to the ACQ1 state upon the detection of a comma.

NOTE:

The Lane Sync bit = '0' bit from any/or all channels will cause a local fault to be output on the receive data bus.

ACQ1

During this state the comma detect circuit is active but code word re-alignment is disabled. The TLK3118 will remain in this state until either a comma is detected in the same code word alignment position as found in state UNSYNC or a decode error is encountered. While in this state, the Lane Sync bit for the particular channel will remain de-asserted indicating the lane is not synchronized. A decode or running disparity error will return the channel state to UNSYNC. A detected comma will cause the channel state to transition to ACQ2.

NOTE:

The Lane Sync bit = '0' will cause a local fault to be output on the receive data bus.

ACQ2

During this state, the comma detect circuit is active but code word re-alignment is disabled. The TLK3118 will remain in this state until either a comma is detected in the same code word alignment position as found in state UNSYNC or a decode error is encountered. While in this state, the Lane Sync bit for the particular channel will remain de-asserted indicating the lane is not synchronized. A decode or running disparity error will return the channel state to UNSYNC. A detected comma will cause the channel state to transition to ACQ3.

ACQ3

During this state the comma detect circuit is active but code word re-alignment is disabled. The TLK3118 will remain in this state until either a comma is detected or a decode error encountered. . While in this state, the Lane Sync bit for the particular channel will remain de-asserted indicating the lane is not synchronized.7 A decode or running disparity error will return the channel state to UNSYNC. A detected comma will cause the channel state to transition to SYNC.

SYNC

This is the normal state for receiving data. When in this state, the TLK3118 will set the Lane Sync bit to '1' for the particular channel in the MDIO register bits 4:5.24.3:0 indicating the lane has been synchronized. During this state the comma detect circuit is active but code word re-alignment is disabled. A decode or running disparity error will cause the channel state to transition to MISS1.

MISS1

When entering this state an internal error counter is cleared. If the next four consecutive codes are decoded without error, the channel state reverts back to SYNC. If a decode or running disparity error is detected, the channel state will transition to MISS2.

MISS2

When entering this state an internal error counter is cleared. If the next four consecutive codes are decoded without error, the channel state reverts back to MISS1. If a decode or running disparity error is detected, the channel state will transition to MISS3.

MISS3

When entering this state an internal error counter is cleared. If the next four consecutive codes are decoded without error, the channel state reverts back to MISS1. If a decode or running disparity error is detected, the channel state will transition to UNSYNC.

End-of-Packet Error Detection

Because of their unique data patterns, /A/ (K28.3), /K/ (K28.5), and /T/ (K29.7) will catch running disparity errors that may have propagated undetected from previous codes in a packet. Running disparity errors detected by these control codes at the end of packets will cause the previous data codes to be reported as errors (0xFE) to allow the protocol device to reject the packet (see Figure 11).

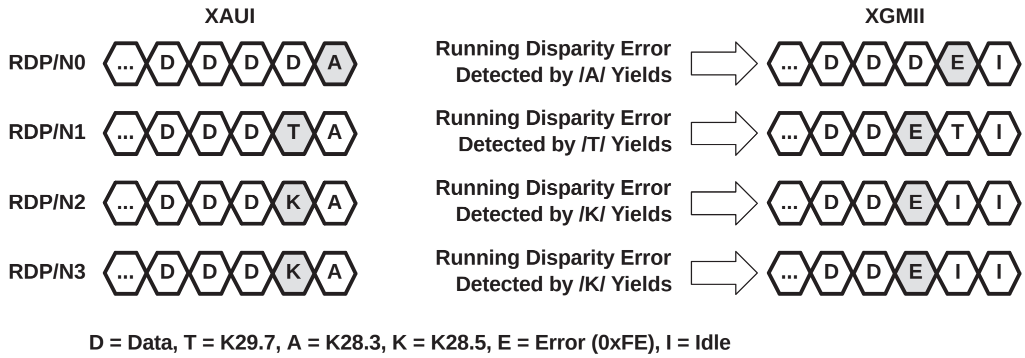


Figure 11. End-of-Packet Error Detection

Fault Detection and Reporting

The TLK3118 will detect and report local faults as well as forward both local and remote faults as defined in the IEEE P802.3ae 10Gbps Ethernet Standard to aid in fault diagnosis. All faults detected by the TLK3118 are reported as local faults to the upper layer protocols. Once a local fault is detected in the TLK3118, MDIO register bit 4:5.1.7 is set. Fault sequences, sequence ordered sets received by the TLK3118, either on the Transmit Data Bus or on the high speed receiver pins, are forwarded without change to the MDIO registers in the TLK3118. Also, note that the TLK3118 is capable of performing CTC operation where only RF and LF or any Q sequences are transported (not generated) in either the transmit or receive direction.

TLK3118 reports a fault by outputting a K28.4 (0x9C) on RXD(7:0), 0x00 on RXD(15:8) and RXD(23:8) and 0x01 for local faults on RXD(31:24). Forwarding of remote faults is handled as a normal transmission. Note that the TLK3118 will not generate a remote fault indication or any other type of Q.

Receive Synchronization and Skew Compensation

Regardless of which mode is selected, the TLK3118 has a FIFO enabled on the receive data path coming from each serial link to compensate for channel skew and clock phase and frequency tolerance differences between the recovered clocks for each channel and the receive output clock RCLK. This FIFO has a depth of 32 locations (32 bits wide for each location).

The de-skew of the 4 serial links that make up each XAUI channel into a single 32 bit wide column of data is accomplished by alignment of the receive FIFO’s on each serial link to a K28.3 control code sent during the inter-packet gap (IPG) between data packets or during initial link synchronization. The K28.3 code (referred to as the “A” or alignment code) is transmitted on the first column following the end of the data packet as shown in Figure 13.

The column de-skew state machine is provided in the following figure. The status of column alignment can be monitored by reading MDIO registers 4:5.24.12 for global alignment or 4:5.24.3:0 for particular channel synchronization.

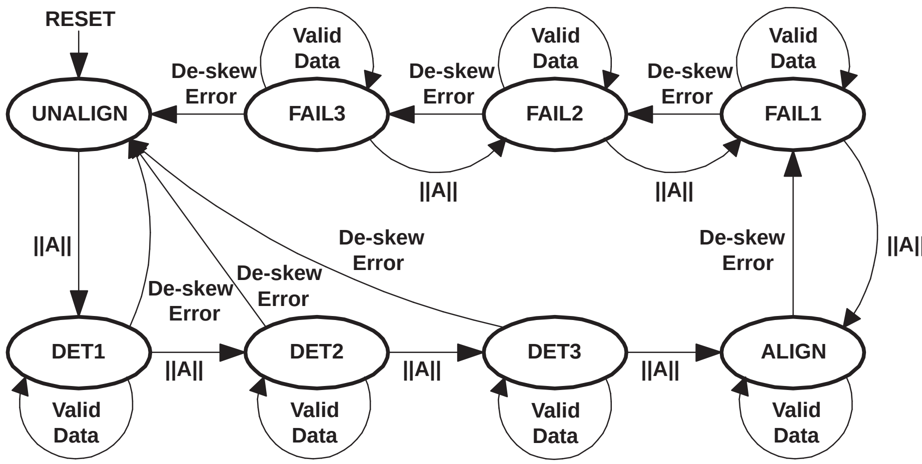


Figure 12. Column De-Skew State Machine

Column State Descriptions

UNALIGN

This is the initial state for the column state machine upon device power up or reset. If any of the channel state machines are set to UNSYNC, the column state is set to UNALIGN. In this state, the column state machine will search for alignment character codes (K28.3 or /A/) on each channel and align the FIFO pointers on each channel to the /A/ character code. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4:5.24.12, indicating the column is not aligned. The column state will transition to the DET1 state upon the detection and alignment of /A/ character codes in all four channels.

DET1

During this state, the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. The column state machine will remain in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels) or a deskew error is detected, the column state machine will transition to state UNALIGN. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4:5.24.12 indicating the column is not aligned. Detection of a complete alignment column will cause the column state machine to transition to state DET2.

NOTE:

The XGXS Lane Alignment bit = '0' will cause a local fault to be output on the receive data bus.

DET2

During this state, the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. The column state machine will remain in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels) or a deskew error is detected, the column state machine will transition to state UNALIGN. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4:5.24.12 indicating the column is not aligned. Detection of a complete alignment column will cause the column state machine to transition to state DET3.

NOTE:

The XGXS Lane Alignment bit = '0' will cause a local fault to be output on the receive data bus.

DET3

During this state, the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. The column state machine will remain in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels) or a deskew error is detected, the column state machine will transition to state UNALIGN. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4:5.24.12 indicating the column is not aligned. Detection of a complete alignment column will cause the column state machine to transition to state ALIGN.

NOTE:

The XGXS Lane Alignment bit = '0' will cause a local fault to be output on the receive data bus.

ALIGN

This is the normal state for receiving data. When in this state, the column state machine will set the Column Alignment Sync bit to '1' in MDIO registers 4:5.24.12 indicating that all channels are aligned. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If a deskew error is detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state FAIL1.

FAIL1

When in this state, the Column Alignment Sync bit is '1' in MDIO registers 4:5.24.12. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If a complete alignment column is not detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state FAIL2.

FAIL2

When in this state, the Column Alignment Sync bit is '1' in MDIO registers 4:5.24.12. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If a complete alignment column is not detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state FAIL3.

FAIL3

When in this state, the Column Alignment Sync bit is '1' in MDIO registers 4:5.24.12. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If complete alignment column is not detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state UNALIGN.

Inter-Packet Gap Management

When in transceiver mode, the TLK3118 replaces the idle codes (see Table 2) during the Inter-Packet Gap (IPG) with the necessary codes to perform all channel alignment, byte alignment, and clock tolerance compensation as defined in IEEE 802.3ae 10Gbps Ethernet Standard. According to the Ethernet Standard, a valid packet must begin on TXD(0:7) of the XGMII. However, due to variable packet sizes, the IPG can begin on any channel. The TLK3118 will replace idle codes latched on the same XGMII clock edge as the end of packet code with /K/ codes (as shown in Figure 13).

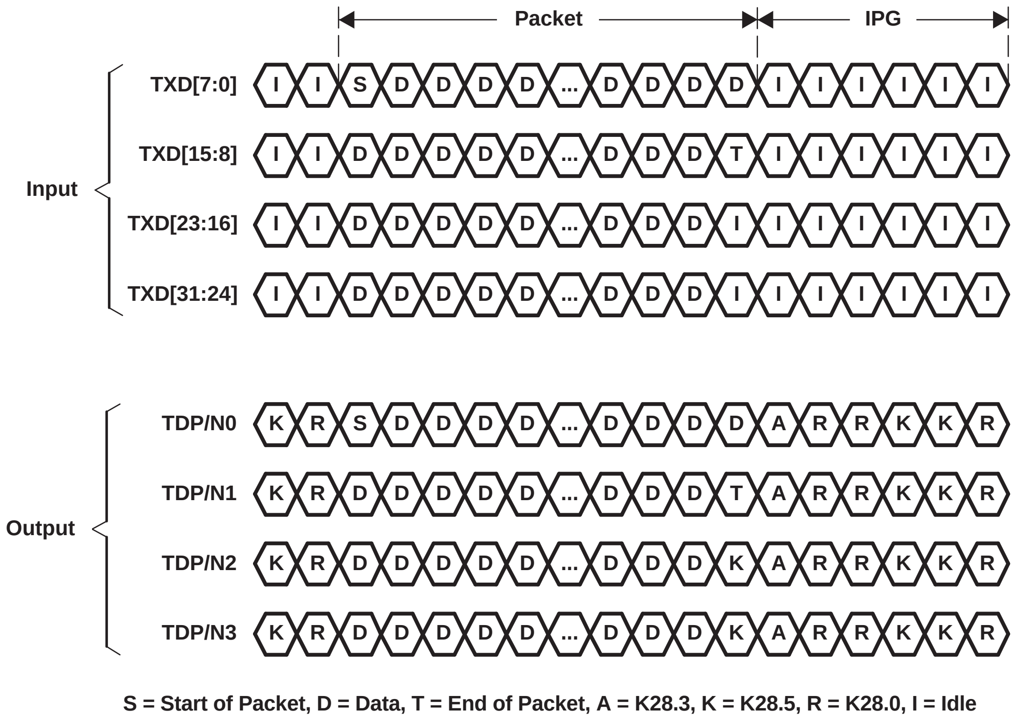


Figure 13. Inter-Packet Gap Management

The subsequent idles in the IPG will be replaced by “columns” of channel alignment codes (K28.3), byte alignment codes (K28.5), or clock tolerance compensation codes (K28.0). The state machine which governs the IPG replacement procedure is illustrated in Figure 14, with notation defined in Table 2. Note that any IPG management state will transition to send data if the IPG is terminated.

The repetition of the “/A/” pattern on each serial channel allows the FIFO’s to remove or add the required phase and frequency difference to align the data from all four serial links of a XAUI channel and allow output of the aligned 32 bit wide data on a single edge of the receive clock, RCLK, as shown in Figure 15.

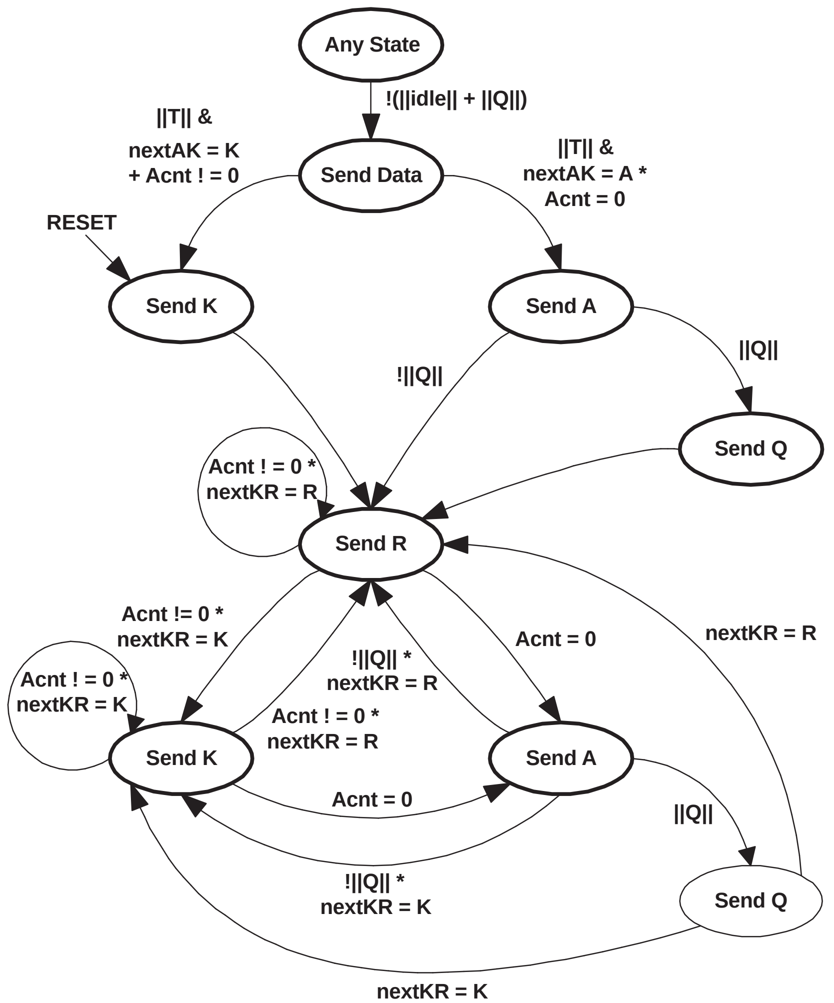


Figure 14. IPG Management State Machine

Table 4. IPG Management State Machine Notation

Symbol	Definition
||idle||	XGMII idle. 0x07 on TXD(x:: :x-7),
||Q||	Link status message: K28.4, Dx.y, Dx.y, Dx.y.
nextAK	A Boolean variable. It takes the value K when an A is sent at the beginning of the IPG and the value A when a K is sent at the beginning of the IPG. Its initial value is K.
Acnt	When an A character is sent, variable Acnt is loaded with a random number such that 16 ≤ Acnt ≤ 31. Acnt is decremented each time a column of A characters is generated.
nextKR	A randomly-generated Boolean that can assume the value K or R.
||T||	Terminate Character Column (Terminate Character in Any Lane).

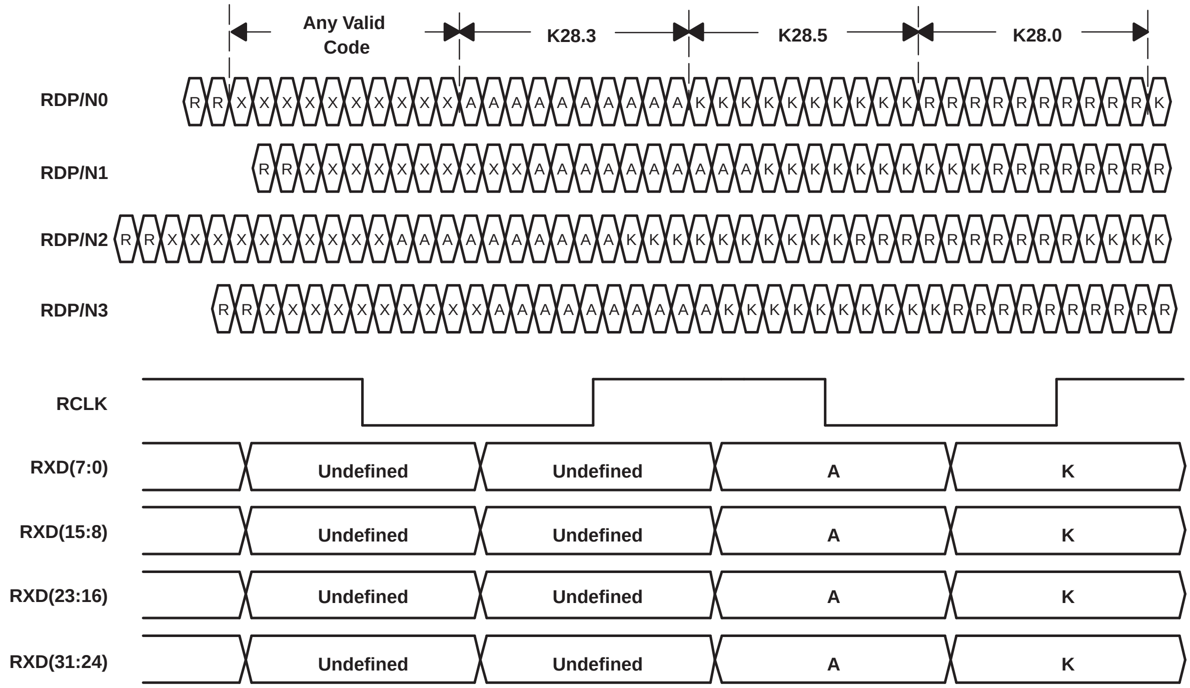


Figure 15. Channel Synchronization Using Alignment Code

Clock Tolerance Compensation (CTC)

The XAUI interface is defined to allow for separate clock domains on each side of the link. If the reference clocks difference for two devices on a XAUI link is not compensated for, it will lead to over or under run of the FIFO's on the receive/transmit data path. The TLK3118 provides compensation for these differences in clock frequencies via the insertion or the removal of /R/ characters on all channels, as shown in Figure 16 and Figure 17.

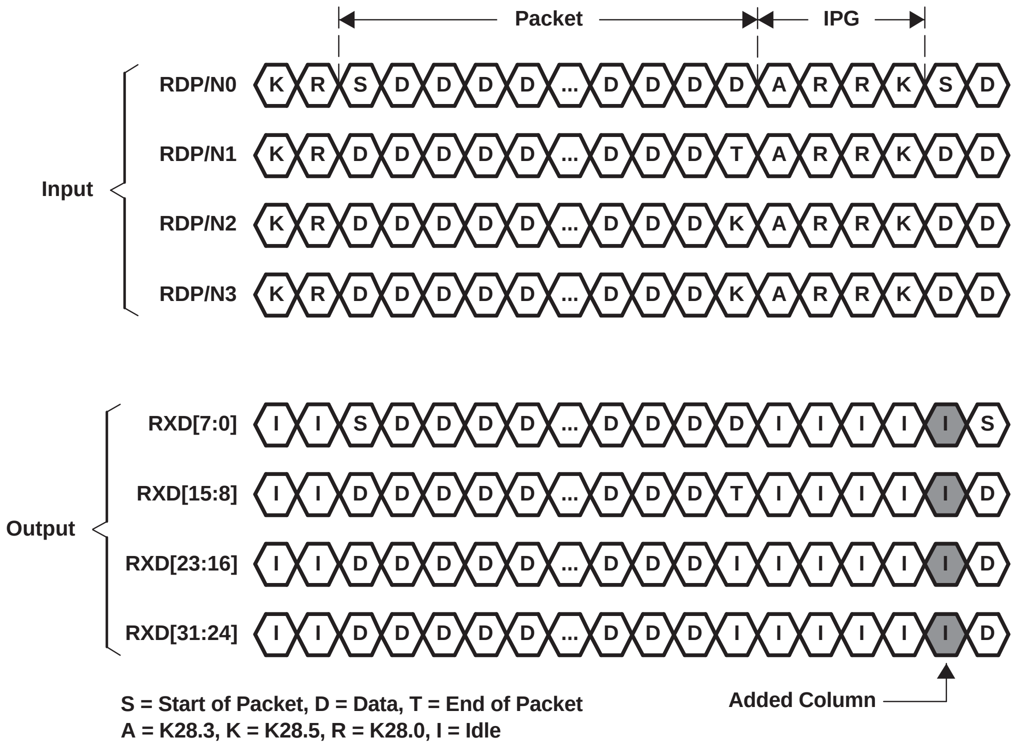


Figure 16. Clock Tolerance Compensation: Add

The /R/ code is disparity neutral, allowing its removal or insertion without affecting the current running disparity of each channel's serial stream.

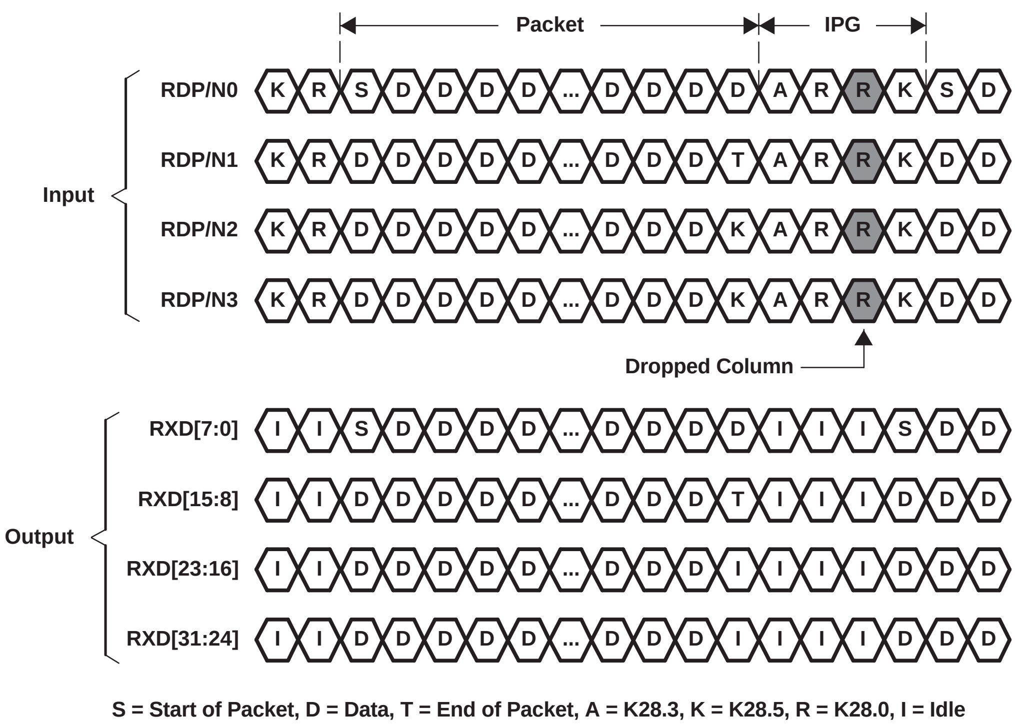


Figure 17. Clock Tolerance Compensation: Drop

Parallel to Serial

The parallel-to-serial shift register on each channel takes in data and converts it to a serial stream. The shift register is clocked by the internally generated bit clock, which is 10 times the reference clock (REFCLKP/REFCLKN) frequency. The least significant bit (LSB) for each channel is transmitted first.

Serial to Parallel

For each channel, serial data is received on the RDPx/RDNx pins. The interpolator and clock recovery circuit will lock to the data stream if the clock to be recovered is within ±200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. If enabled, the 10-bit wide parallel data is then fed into 8b/10b decoders.

High-Speed CML Output

The high speed data output driver is implemented using Current Mode Logic (CML) with integrated pull up resistors requires no external components. The line must be AC coupled.

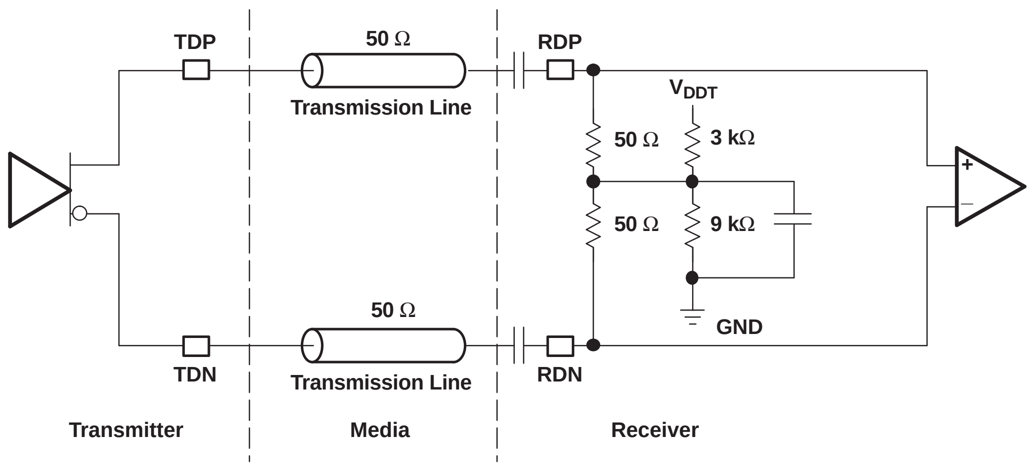


Figure 18. Example High Speed I/O AC Coupled Mode

Standard Current Mode Logic (CML) drivers usually require external components. The disadvantage of the external edge control is a limited edge rate due to package and line parasitic. The CML driver on TLK3118 has on-chip 50-Ω termination resistors terminated to VDDT therefore provides optimum performance for increased speed requirements. The transmitter output driver is highly configurable allowing, output amplitude and pre-emphasis to be turned to a channel's individual requirements. An internal voltage reference derived from VDDT is also available to provide the target for output amplitude control loop. This reference is enabled by holding register bit 4/5.32900.6 low and will result in a nominal output amplitude of ~1010mV differential pk-pk for 100% swing. The receiver input is internally biased to 2×VDDT/3, which is the optimum voltage for input sensitivity. As the input and output references are derived from VDDT, the tolerance of this supply will dominate the accuracy of the internal reference. Applications requiring higher tolerance output amplitude are advised to provide a high accuracy external reference.

When transmitting data across long lengths of PCB trace or cable, the high frequency content of the signal is attenuated due to the skin effect of the media. This causes a “smearing” of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, 2-tap finite impulse response (FIR) transmit pre-emphasis is implemented. In a 1-tap FIR pre-emphasis, differential swing is increased or “pre-emphasized” for the bit immediately following a transition and subsequently reduced or “de-emphasized” for run lengths greater than one, as shown in Figure 19. This provides additional high frequency energy to compensate for PCB or cable loss.

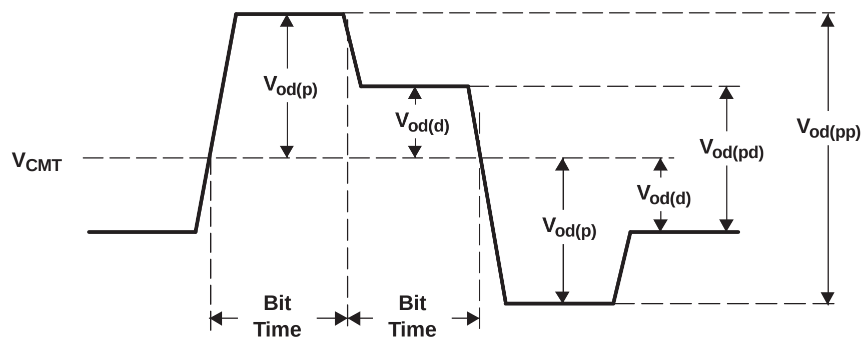


Figure 19. Output Differential Voltage with 1-Tap FIR Pre-Emphasis

The 2-stage mode operates in a similar manner but considers the logic level of the previous two transmitted bits when determined how much pre-emphasis to apply. The level and mode of the pre-emphasis is programmable via MDIO Register bits 4/5.32900.14:11. Users can control the strength of the pre-emphasis to optimize for a specific system requirement.

High-Speed Receiver

The high speed receiver is conformed to the physical layer requirements of IEEE 802.3ae Clause 47(XAUI), Gigabit Ethernet, and Fiber channel 1 and 2. The termination impedances of the receiver is configured as 100Ω with the center tap weakly tied to 2×VDDT/3 with a capacitor to create an AC ground. AC coupling is always required on receiver inputs.

All receive channels incorporate an adaptive equalizer. This circuit compensates for channel insertion loss by amplifying the high frequency components of the signal, reducing inter-symbol interference. Setting 4/5.32900.2 will enable adaptive equalization. In this mode, both the gain and bandwidth of the equalizer with be controlled by the receiver equalization logic. Bandwidth selection will be based on the setting applied to 4/5.32901.14:13 and 4/5.32900.3. Equalization can be disabled by setting 4/5.32900.2 low.

Loopback

Two internal loopback modes are possible for each XAUI Channel Group A and B. One, called XGMII loopback, allows the transmit 10 bit data to be looped back to the receive 10 bit data inputs. The other, called XAUI loopback, allows the receive XGMII data to be looped back to the transmit data path. These configurations are listed in Table 5.

Table 5. Loopback Configuration

RETIM	4/5.0.14	4/5.32792.1	4/5.32792.0	Configuration
0	0	0	0	Transceiver Mode — Normal Operation
1	X	X	X	Retime Mode(XAUI A receiver data is routed out to XAUI B. XAUI B receiver data is routed to XAUI A)
0	1	X	X	If configured as PHY XS, XAUI is loopback to the same channel. If configured as DTE XS, XGMII is loopback to the same channel.
0	0	1	0	XAUI data loopback
0	0	0	1	XGMII data loopback

An external loopback (requiring external connection) is also supported, which can be used with the PRBS patterns, as well as the CJPAT, CRPAT, Mixed/High/Low Frequency tests.

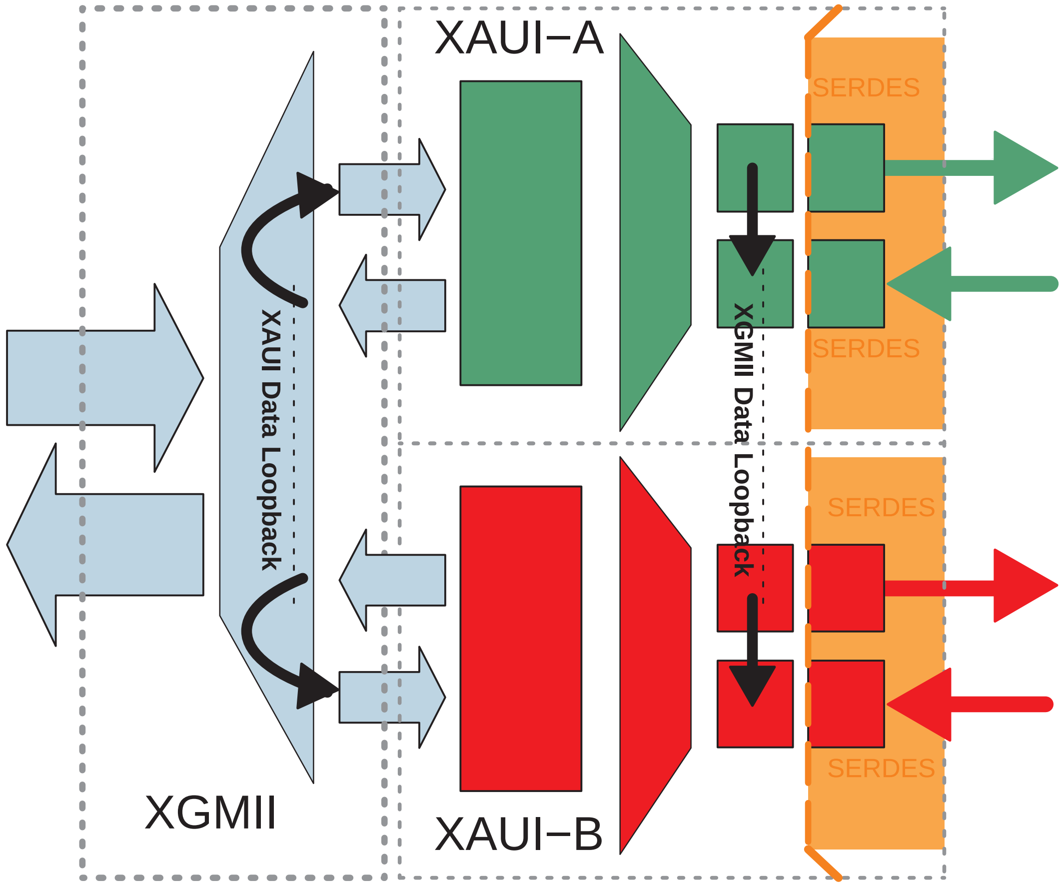


Figure 20. Data Loopback

XGMII Bus Buffers

The XGMII bus is implemented using 1.5-V HSTL buffer in compliance with JEDEC 1.5-V standard JESD8-6 with VTP-controlled driver, receiver and an optional termination. The VTP macro function is to adjust the HSTL buffer output impedance to match the external resistors. (In this case 50 Ω)

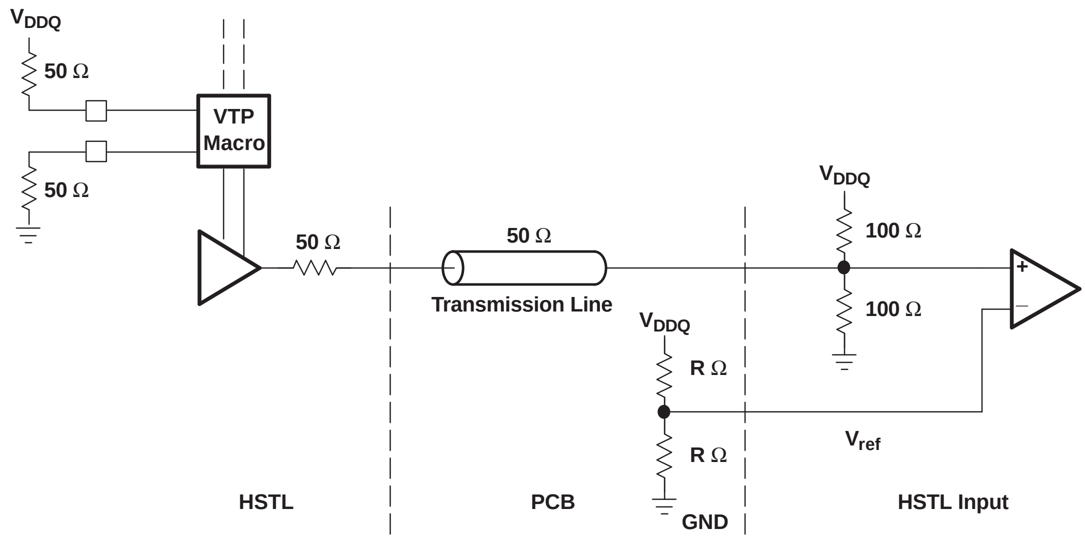


Figure 21. XGMII Bus Buffers

Link Test Functions

The TLK3118 has an extensive suite of built in test functions to support system diagnostic requirements. Each channel has built-in link test generator and verification logic. Several patterns can be selected via the MDIO that offer extensive test coverage. The patterns are: 2^7-1 or 2^{23}-1 PRBS (Pseudo Random Binary Sequence), CJPAT, CRPAT, high and low and mixed frequency patterns.

MDIO Management Interface

The TLK3118 supports the Management Data Input/Output (MDIO) Interface as defined in Clauses 45 of the IEEE 802.3ae Ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK3118 is possible without use of this interface since all of the essential signals necessary for operations are accessible via the device pins. However, some additional features are accessible only through the MDIO.

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The device address is defined by the external inputs DVAD (4:1). DVAD (0) indicates whether the device is responding as a DTE (5.xxx) (DVAD (0) = 1) or PHY (4.xxx) (DVAD (0) = 0). Note that each register is accessed as either DTE or PHY devices in the TLK3118; although physically there is only one register accessed two different ways. Also note, the XAUI interfaces must both be DTE devices or both be PHY devices. An even PHY Address (as shown below) indicates an access to XAUI A register space, and an odd PHY Address indicates access to XAUI B register space.

Write transactions which address an invalid register or device or a read only register will be ignored. Read transactions which address an invalid register or device will return a 0.

NOTE:

Registers from address 32900 and above can be accessed from A side or B side. These registers are implemented from the top level and can control the entire device (XAUI-A & XAUI-B).

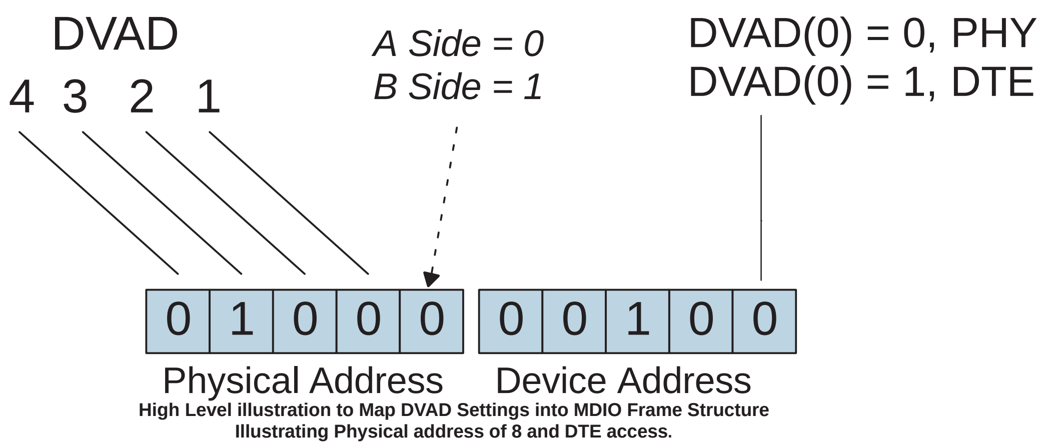


Figure 22. Device Address

Timing for an address transaction is shown in Figure 23. The timing required to write to the internal registers is shown in Figure 24. The timing required to read from the internal registers is shown in Figure 25. The timing required to read from the internal registers and then increment the active address for the next transaction is shown in Figure 26.

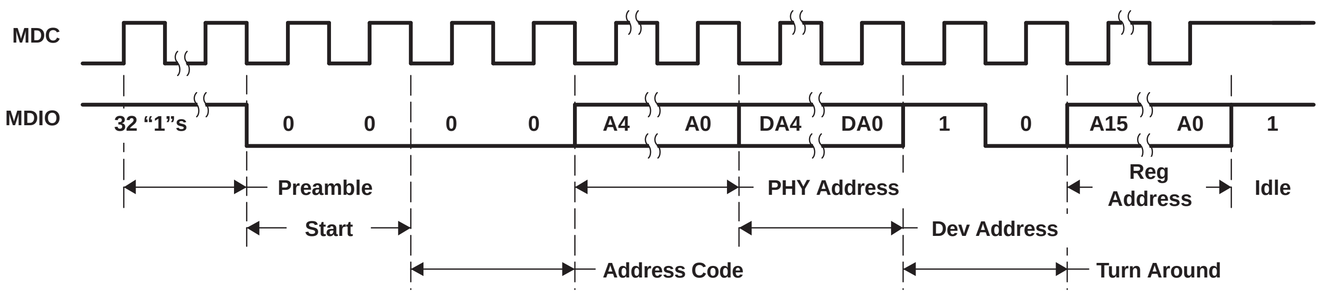


Figure 23. Management Interface Extended Space Address Timing

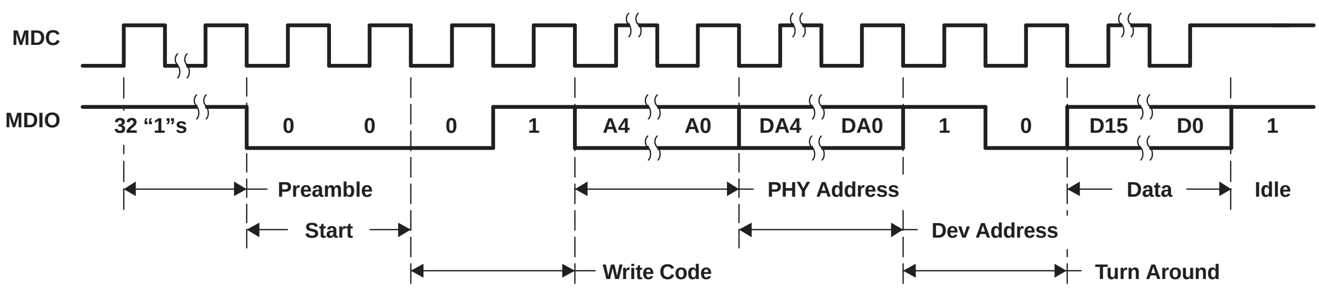


Figure 24. Management Interface Extended Space Write Timing

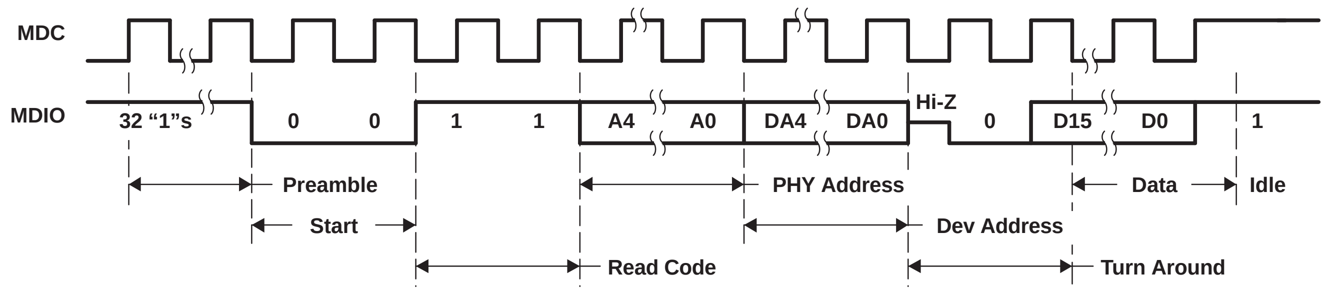


Figure 25. Management Interface Extended Space Read Timing

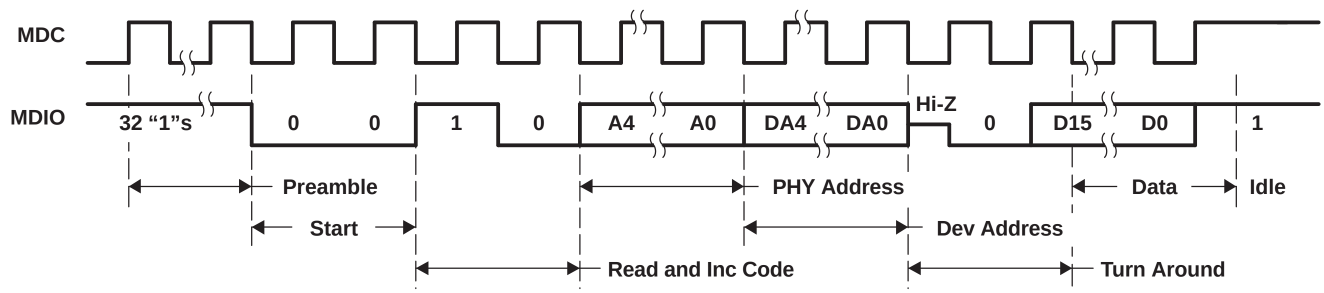


Figure 26. Management Interface Extended Space Read and Increment Timing

The IEEE 802.3 Clause 45 specification defines many of the registers, and additional registers have been implemented for expanded functionality.

PROGRAMMER'S REFERENCE

Table 6. XS[(1)]_CONTROL_1

Address:0x0000		Default:0x2040	
Bit(s)	**Name**	**Description**	**Access[(2)]**
4/5.0.15	Reset	1 = XS reset (including all registers) 0 = Normal operation	RW SC
4/5.0.14	Loop back	1 = Enable loop back mode. If the device is configured as PHY XS (DVAD(0) = 0), then XAUI_LOOPBACK will be performed (RX parallel to TX parallel) If the device is configured as DTE XS (DVAD(0) = 1), then XGMII_LOOPBACK will be performed (TX serial to RX serial) 0 = Disable loop back mode	RW
4/5.0.13	Speed Selection	This bit always reads 1 indicating operation at 10 Gb/s and above.	
4/5.0.11	Low power	1 = Low power mode 0 = Normal operation	
4/5.0.6	Speed Selection	This bit always reads 1 indicating operation at 10Gbps and above.	
4/5.0.5:2	Speed Selection	These bits always read 0 indicating operation at 10Gbps.	

(1) In this section XS refers to either PHY or DTE XS device.
(2) RO: Read-Only , RW: Read-Write, SC: Self-Clearing, LL: Latching-Low, LH: Latching-High, COR: Clear-on-Read

Table 7. XS_STATUS_1

Address:0x0001		Default:0x0082	
Bit(s)	**Name**	**Description**	**Access**
4/5.1.7	Fault	1 = Fault condition detected (either on TX or RX side. This bit is ORed version of 4/5.8.10 and 4/5.8.11) 0 = No fault condition detected	RO

Table 7. XS_STATUS_1 (continued)

Address:0x0001		Default:0x0082	
Bit(s)	**Name**	**Description**	**Access**
4/5.1.2	XS Transmit Link Status	1 = XS Transmit link is up 0 = XS Transmit links is down (This bit is latched low version of 4/5.24.12)	RO/LL
4/5.1.1	Low Power Ability	This bit always reads 1 indicating support for low power mode	RO

Table 8. XS_DEVICE_IDENTIFIER_1

Address:0x0002		Default:0x4000	
Bit(s)	**Name**	**Description**	**Access**
4/5.2.15.0	OUI c:r	Organizationally unique identifier.	RO

Table 9. XS_DEVICE_IDENTIFIER_2

Address:0x003		Default:0x50B0	
Bit(s)	**Name**	**Description**	**Access**
4/5.3.15:0	OUI c:r	Device identifier. Manufacturer model and revision number	RO

Table 10. XS_SPEED_ABILITY

Address:0x004		Default:0x0001	
Bit(s)	**Name**	**Description**	**Access**
4/5.4.0	10G Capable	This bit always reads 1 indicating operation at 10Gb/s	RO

Table 11. XS_DEVICES_IN_PACKAGE_1

Address:0x0005		Default:0x0010	
Bit(s)	**Name**	**Description**	**Access**
4/5.5.5	DTE XS Present	1 = DTE XS present in the package 0 = DTE XS not present in the package Read will return 1, when dvad_in is high	RO
4/5.5.4	PHY XS Present	1 = PHY XS present in the package 0 = PHY XS not present in the package Read will return 1, when dvad_in is low	
4/5.5.3	PCS Present	Always reads 0	
4/5.5.2	WIS Present	Always reads 0	
4/5.5.1	PMD/PMA Present	Always reads 0	
4/5.5.0	Clause 22 registers Present	Always reads 0	

Table 12. XS_DEVICES_IN_PACKAGE_2

Address:0x0006		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.6.15	Vendor Specific Device 2 Present	This bit always reads 0 indicating that vendor specific device 2 not present in package	RO
4/5.6.14	Vendor Specific Device 1 Present	This bit always reads 0 indicating that vendor specific device 1 not present in package	

Table 13. XS_STATUS_2

Address:0x0008		Default:0x8C00	
Bit(s)	**Name**	**Description**	**Access**
4/5.8.15:14	Device present	Always read 10 indicating that device responds at this address	RO

Table 13. XS_STATUS_2 (continued)

Address:0x0008		Default:0x8C00	
Bit(s)	**Name**	**Description**	**Access**
4/5.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
4/5.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	

Table 14. XS_PACKAGE_IDENTIFIER_1

Address:0x000E		Default:0x4000	
Bit(s)	**Name**	**Description**	**Access**
4/5.14.15:0	OUI c:r	Organizationally unique identifier.	RO

Table 15. XS_PACKAGE_IDENTIFIER_2

Address:0x000F		Default:0x50B0	
Bit(s)	**Name**	**Description**	**Access**
4/5.15.15:0	OUI c:r	Organizationally unique identifier Manufacturer model and revision number.	RO

Table 16. XS_LANE_STATUS

Address:0x0018		Default:0x0C00	
Bit(s)	**Name**	**Description**	**Access**
4/5.24.12	Align status	When 1, indicates all lanes are aligned	RO
4/5.24.11	Pattern testing ability	Always reads 1. Able to generate test patterns	
4/5.24.10	Loopback ability	Always read 1. Has the ability to perform loopback function	
4/5.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	
4/5.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	
4/5.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	
4/5.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	

Table 17. XS_TEST_CONTROL

Address:0x0019		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.25.2	Receive test-pattern enable	When 1, indicates test pattern function is enabled.	RW
4/5.25.1:0	Test-pattern select	00 = High frequency test pattern 01 = Low frequency test pattern 10 = Mixed frequency test pattern 11 = Reserved	

Table 18. TEST_CONFIG

Address:0x8000		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32768.1	CRPAT enable	When set, enables the CRPAT test pattern on all 4 lanes.	RW
4/5.32768.0	CJPAT enable	When set, enables the CJPAT test pattern on all 4 lanes.	

Table 19. 9.4.1 TEST_VERIFICATION_CONTROL

Address:0x8001		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32769.1	CRPAT check enable	When set, enables the verification of CRPAT test modes.	RW
4/5.32769.0	CJPAT check enable	When set, enables the verification of CJPAT test modes.	

Table 20. TX_FIFO_STATUS

Address:0x8002		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32770.9	Lane 3 overflow	When high, indicates that transmit FIFO overflow condition occurred for the corresponding lane.	RO/LH
4/5.32770.8	Lane 2 overflow		
4/5.32770.7	Lane 1 overflow		
4/5.32770.6	Lane 0 overflow		
4/5.32770.5	Lane 3 underflow	When high, indicates that transmit FIFO underflow condition occurred for the corresponding lane.	
4/5.32770.4	Lane 2 underflow		
4/5.32770.3	Lane 1 underflow		
4/5.32770.2	Lane 0 underflow		
4/5.32770.1	Overflow	When high, indicates that transmit FIFO overflow condition occurred in any lane	
4/5.32770.0	Underflow	When high, indicates that transmit FIFO underflow condition occurred in any lane	

Table 21. TX_FIFO_DROP_COUNT

Address:0x8003		Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32771.15:0	Drop count	Counter for number of idle drops in the transmit FIFO	RO/COR

Table 22. TX_FIFO_INSERT_COUNT

Address:0x8004		Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32772.15:0	Insert count	Counter for number of idle inserts in the transmit FIFO	RO/COR

Table 23. TX_CODEGEN_STATUS

Address:		Default:	
Bit(s)	**Name**	**Description**	**Access**
4/5.32773.6	Invalid XGMII character in lane 3	When high, indicates invalid XGMII character received in the corresponding lane.	RO/LH
4/5.32773.5	Invalid XGMII character in lane 2		
4/5.32773.4	Invalid XGMII character in lane 1		
4/5.32773.3	Invalid XGMII character in lane 0		
4/5.32773.2	Invalid XGMII character error	When high, indicates invalid XGMII character received in any lane	
4/5.32773.1	Invalid T column error	When high, indicates invalid Terminate column (column that contains Terminate character not followed by Idle character(s)) received from the XGMII interface.	
4/5.32773.0	Invalid S column error	When high, indicates invalid Start column (column that contains Start character in a lane other than lane 0) received from the XGMII interface.	

Table 24. LANE_0_TEST_ERROR_COUNT

Address:0x8006		Default:0xFFFD	
Bit(s)	Name	Description	Access
4/5.32774.15:0	Lane 0 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 0. This counter increments by one for each received character that has error.	RO/COR

Table 25. LANE_1_ TEST_ERROR_COUNT

Address:0x8007		Default:0xFFFD	
Bit(s)	Name	Description	Access
4/5.32775.15:0	Lane 1 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 1. This counter increments by one for each received character that has error.	RO/COR

Table 26. LANE_2_ TEST_ERROR_COUNT

Address:0x8008		Default:0xFFFD	
Bit(s)	Name	Description	Access
4/5.32776.15:0	Lane 2 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 2. This counter increments by one for each received character that has error.	RO/COR

Table 27. LANE_3_ TEST_ERROR_COUNT

Address:0x8009		Default:0xFFFD	
Bit(s)	Name	Description	Access
4/5.32777.15:0	Lane 3 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 3. This counter increments by one for each received character that has error.	RO/COR

Table 28. CRPAT_CJPAT_TEST_ERROR_COUNT_1 (1)

Address:0x800A		Default:0xFFFF	
Bit(s)	Name	Description	Access
4/5.32778.15:0	CRPAT/CJPAT test error counter	MSB of CRPAT/CJPAT error counter for all 4 lanes	RO

(1) User has to make sure that register 32778 is read first and then register 32779. If user reads register 32779 without reading register 32778 first, then the count value read through 32779 register may not be correct.

Table 29. CRPAT_CJPAT_TEST_ERROR_COUNT_2 (1)

Address:0x800B		Default:0xFFFD	
Bit(s)	Name	Description	Access
4/5.32779.15:0	CRPAT/CJPAT test error counter	LSB of CRPAT/CJPAT error counter for all 4 lanes	RO

(1) User has to make sure that register 32778 is read first and then register 32779. If user reads register 32779 without reading register 32778 first, then the count value read through 32779 register may not be correct.

Table 30. LANE_0_EOP_ERROR_COUNT(1)

Address:0x800C			Default:0xFFFD
Bit(s)	**Name**	**Description**	**Access**
4/5.32780.15:0	Lane 0 end of packet error counter	End of packet termination error counter for lane 0. End of packet error for lane 0 is detected on the RX side. It is detected when Terminate character is in lane 0 and one or both of the following holds: • Terminate character is not followed by /K/ characters in lanes 1, 2 and 3 • The column following the terminate column is neither ||K|| or ||A||.	RO/COR

(1) Counter will increment by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 31. LANE_1_EOP_ERROR_COUNT(1)

Address:0x800D			Default:0xFFFD
Bit(s)	**Name**	**Description**	**Access**
4/5.32781.15:0	Lane 1 end of packet error counter	End of packet termination error counter for lane 1. End of packet error for lane 1 is detected on the RX side. It is detected when Terminate character is in lane 1 and one or both of the following holds: • Terminate character is not followed by /K/ characters in lanes 2 and 3 • The column following the terminate column is neither ||K|| or ||A||.	RO/COR

(1) Counter will increment by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 32. LANE_2_EOP_ERROR_COUNT(1)

Address:0x800E			Default:0xFFFD
Bit(s)	**Name**	**Description**	**Access**
4/5.32782.15:0	Lane 2 end of packet error counter	End of packet termination error counter for lane 2. End of packet error for lane 2 is detected on the RX side. It is detected when Terminate character is in lane 2 and one or both of the following holds: • Terminate character is not followed by /K/ character in lane 3 • The column following the terminate column is neither ||K|| or ||A||.	RO/COR

(1) Counter will increment by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 33. LANE_3_EOP_ERROR_COUNT(1)

Address:0x800F			Default:0xFFFD
Bit(s)	**Name**	**Description**	**Access**
4/5.32783.15:0	Lane 3 end of packet error counter	End of packet termination error counter for lane 3. End of packet error for lane 3 is detected on the RX side. It is detected when Terminate character is in lane 3 and the column following the terminate column is neither ||K|| or ||A||.	RO/COR

(1) Counter will increment by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 34. LANE_0_CODE_ERROR_COUNT(1)

Address:0x8010			Default:0xFFFD
Bit(s)	**Name**	**Description**	**Access**
4/5.32784.15:0	Lane 0 code error counter	Output 16-bit counter for invalid code group found in lane 0. Invalid code group is detected when the 8B10B decoder cannot decode the received codeword.	RO/COR

(1) Counter will increment by 1 when codeword error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 35. LANE_1_CODE_ERROR_COUNT[(1)]

Address:0x8011			Default:0xFFFD
Bit(s)	**Name**	**Description**	**Access**
4/5.32785.15:0	Lane 1 code error counter	Output 16-bit counter for invalid code group found in lane 1. Invalid code group is detected when the 8B10B decoder cannot decode the received codeword.	RO/COR

(1) Counter will increment by 1 when codeword error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 36. LANE_2_CODE_ERROR_COUNT[(1)]

Address:0x8012			Default:0xFFFD
Bit(s)	**Name**	**Description**	**Access**
4/5.32786.15:0	Lane 2 code error counter	Output 16-bit counter for invalid code group found in lane 2. Invalid code group is detected when the 8B10B decoder cannot decode the received codeword.	RO/COR

(1) Counter will increment by 1 when codeword error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 37. LANE_3_CODE_ERROR_COUNT[(1)]

Address:0x8013			Default:0xFFFD
Bit(s)	**Name**	**Description**	**Access**
4/5.32787.15:0	Lane 3 code error counter	Output 16-bit counter for invalid code group found in lane 3. Invalid code group is detected when the 8B10B decoder cannot decode the received codeword.	RO/COR

(1) Counter will increment by 1 when codeword error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 38. RX_CHANNEL_SYNC_STATE

Address:0x8014			Default:0x0000
Bit(s)	**Name**	**Description**	**Access**
4/5.32788.11:9	Channel synchronization FSM state for lane 0	Current state of sync state machine in lane 0	RO
4/5.32788.8:6	Channel synchronization FSM state for lane 1	Current state of sync state machine in lane 1	
4/5.32788.5:3	Channel synchronization FSM state for lane 2	Current state of sync state machine in lane 2	
4/5.32788.2:0	Channel synchronization FSM state for lane 3	Current state of sync state machine in lane 3	

Table 39. RX_LANE_ALIGN_STATUS

Address:0x8015			Default:0x0000
Bit(s)	**Name**	**Description**	**Access**
4/5.32789.15:12	Align state	Current lane alignment FSM state	RO
4/5.32789.0	Lane Alignment FIFO collision	Collision status for lane alignment FIFO. When high, indicates that there is collision error in lane alignment FIFO.	RO/LH

Table 40. RX_CHANNEL_SYNC_STATUS

Address:0x8016			Default:0x0000
Bit(s)	**Name**	**Description**	**Access**
4/5.32790.11	Channel Synchronization status for all lanes	1 = Channel synchronization is achieved in all lanes 0 = Channel synchronization is lost in one or more lanes	RO/LL

Table 41. BIT_ORDER

Address:0x8017		Default:0x0005	
Bit(s)	**Name**	**Description**	**Access**
4/5.32791. 3	XGMII RX bit order	When high, reverses the order of bits in the parallel data sent from XAUI RX A and B for each lane.	RW
4/5.32791. 2	XAUI RX bit order	When high, reverses the order of bits in the parallel data received from SERDES macros for XAUI RX A and B for each lane.	
4/5.32791. 1	XGMII TX bit order	When high, reverses the order of bits in the parallel data received from the XGMII interface each lane.	
4/5.32791. 0	XAUI TX bit order	When high, reverses the order of bits in the parallel data sent to the SERDES TX macro for each lane.	

Table 42. LOOPBACK_CONTROL

Address:0x8018		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32792. 1	XAUI side loopback	When high, loops back 32 bit data and 4 control bits from the RX path to the TX path. (4/5.0.14 should be 0 else no effect)	RW
4/5.32792. 0	XGMII side loopback	When 1, loops back 40 bit data from TX path to the RX path (4/5.0.14 should be 0 else no effect)	

Table 43. TX_BYPASS_CONTROL

Address:0x8019		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32793.15	TX IPG management bypass	When high, disables IPG management (replacing Idle XGMII characters with /A/K/R/Q/ code-words) in transmit side.	RW
4/5.32793.11	TX CTC Bypass	When high, disables clock tolerance compensation in transmit side	
4/5.32793.7	Lane 3 8B10B encoder bypass	When high, disables 8B10B encoding on the corresponding lane	
4/5.32793.6	Lane 2 8B10B encoder bypass		
4/5.32793.5	Lane 1 8B10B encoder bypass		
4/5.32793.4	Lane 0 8B10B encoder bypass		

Table 44. RX_CTC_STATUS

Address:0x801A		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32794.9	Lane 3 overflow	When high, indicates overflow error in the corresponding lane.	RO/LH
4/5.32794.8	Lane 2 overflow		
4/5.32794.7	Lane 1 overflow		
4/5.32794.6	Lane 0 overflow		
4/5.32794.5	Lane 3 underflow	When high, indicates underflow error in the corresponding lane.	
4/5.32794.4	Lane 2 underflow		
4/5.32794.3	Lane 1 underflow		
4/5.32794.2	Lane 0 underflow		
4/5.32794.1	Overflow	When high, indicates overflow error in any lane.	
4/5.32794.0	Underflow	When high, indicates underflow error in any lane.	

Table 45. RX_CTC_INSERT_COUNT

Address:0x801B		Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32795.15:0	Idle insert count	Counter for number of idle insertions in RX side	RO/COR

Table 46. RX_CTC_DELETE_COUNT

Address:0x801C		Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32796.15:0	Idle delete count	Counter for number of idle deletions	RO/COR

Table 47. DATA_DOWN

Address:0x81D		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32797.3	Lane 3 data down	When high, indicates that link for the corresponding lane was inactive (data did not toggle) for 4095 cycles of 312.5-MHz clock. The 312.5 MHz is generated internally by the PLL from the 156-MHz Reference clock.	RO/COR
4/5.32797.2	Lane 2 data down		
4/5.32797.1	Lane 1 data down		
4/5.32797.0	Lane 0 data down		

Table 48. RX_BYPASS_CONTROL

Address:0x801E		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32798.15	RX CTC bypass	When set, bypasses clock tolerance compensation on the RX side	RW
4/5.32798.14	IPG Checker bypass	When set, bypasses the replacement of /A/K/R/ into Idles and also bypasses end-of-packet error checking.	
4/5.32798.11	Lane 3 8B/10B decoder bypass	When set, disables the 8B/10B decoding for the corresponding lane	
4/5.32798.10	Lane 2 8B/10B decoder bypass		
4/5.32798.9	Lane 1 8B/10B decoder bypass		
4/5.32798.8	Lane 0 8B/10B decoder bypass		
4/5.32798.7	Consider sequence column part of IPG	When set, sequence columns are counted as part of IPG When low, sequence columns are not counted as IPG	
4/5.32798.3	RX Lane align bypass	When set, bypasses lane alignment on the RX side	

Table 49. CLOCK_DOWN_STATUS

Address:0x801F		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32799. 7	Lane 3 clock 312 down	When high, indicates that 312-MHz clock is down on the corresponding lane for 255 or more cycles. The detection is done on the transmit side. The 312.5MHz is generated internally by the PLL from the 156-MHz Reference clock.	RO/LH
4/5.32799. 6	Lane 2 clock 312 down		
4/5.32799. 5	Lane 1 clock 312 down		
4/5.32799. 4	Lane 0 clock 312 down		
4/5.32799. 3	Lane 3 clock 156 down	When high, indicates that 156-MHz XGMII clock is down on the corresponding lane for 255 or more cycles. The detection is done on the transmit side.	
4/5.32799. 2	Lane 2 clock 156 down		
4/5.32799. 1	Lane 1 clock 156 down		
4/5.32799. 0	Lane 0 clock 156 down		

Table 50. AUXILIARY_RESET_CONTROL

Address:0x8020		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32800. 15	Transmit auxiliary reset	When set, resets XAUI transmit data path but does not reset any R/W registers.	RW/SC
4/5.32800. 14	Receive auxiliary reset	When set, resets XAUI receive data path but does not reset any R/W registers.	
4/5.32800. 13	TLK3118 auxiliary reset	When set, resets the DDR, RETIME muxing, A/B muxing logic but does not reset any R/W registers.	

Table 51. TEST_PATTERN_STATUS

Address:0x8021		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5/32801.15	Test pattern sync status	When high, indicates that preamble for CRPAT/CJPAT has been recovered.	RO

Table 52. LANE_0_ERROR_CODE

Address:0x8022		Default:0xCE00	
Bit(s)	**Name**	**Description**	**Access**
4/5.32802.15: 7	Lane 0 error code select	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 0 corresponds to 8'h9C with the control bit being 1'b1. The default values for lanes 0~3 correspond to ||LF||	RW

Table 53. LANE_1_ERROR_CODE

Address:0x8023		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32803.15: 7	Lane 1 error code select	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 1 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 54. LANE_2_ERROR_CODE

Address:0x8024		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32804.15: 7	Lane 2 error code select	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 2 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 55. LANE_3_ERROR_CODE

Address:0x8025		Default:0x0800	
Bit(s)	**Name**	**Description**	**Access**
4/5.32805.15: 7	Lane 3 error code select	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 3 corresponds to 8'h01 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 56. RX_PHASE_SHIFT_CONTROL

Address:0x8026		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32806. 15	Lane 3 phase shift	When set, delays the RX data sent to the XGMII interface by one clock cycle	RW
4/5.32806. 14	Lane 2 phase shift		
4/5.32806. 13	Lane 1 phase shift		
4/5.32806. 12	Lane 0 phase shift		

Table 57. CHANNEL_SYNC_CONTROL

Address:0x8027		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32807. 15	Lane 3 channel sync bypass	When set, lane synchronization for the corresponding lane is bypassed.	RW
4/5.32807. 14	Lane 2 channel sync bypass		
4/5.32807. 13	Lane 1 channel sync bypass		
4/5.32807. 12	Lane 0 channel sync bypass		
4/5.32807. 11	Lane 3 channel sync freeze	When set, freezes the last acquired word alignment for the corresponding lane.	
4/5.32807. 10	Lane 2 channel sync freeze		
4/5.32807. 9	Lane 1 channel sync freeze		
4/5.32807. 8	Lane 0 channel sync freeze		

Table 58. SERDES_CONFIG_1 (1)

Address:0x8084			Default:0x802C
Bit(s)	**Name**	**Description**	**Access**
4/5.32900.15	TXBCLKM CFG[23]	0 = Individual lane TXBCLK ports are used 1 =TXBCLK[1] is used to time TD for all lanes (default)	RW
4/5.32900.14:11	Pre emphasis (CFG[22:19])	Refer **Table 59: Transmit Pre-emphasis Settings** Depends on transmit swing setting controlled by CFG [18:17]. These bits do not have any effect if CFG[18:17] = 2'b10 (Default 4'b0000)	
4/5.32900.10:9	SWING (CFG[18:17])	Output swing setting 00 = Maximum transmit amplitude, pre-emphasis available (Default) 01 = 62.5% transmit amplitude, increased pre-emphasis available 10 = 37.5% transmit amplitude, pre-emphasis unavailable 11 = 0% transmit amplitude	
4/5.32900.8:7	Slew Rate (CFG[16:15])	Slew Rate setting Refer **Table 60: Slew rate control. Tx Rise and Fall times** 00 = Fastest edge rate, independent of DATARATE (Default) 01 = Intermediate edge rate for given DATARATE 10 = Slower intermediate edge rate for given DATARATE 11 = Slowest edge rate for given DATARATE	
4/5.32900.6	EXTREF (CFG[14])	0 = Internally generated reference is used to set output amplitude 1 = External reference VREF is used to set output amplitude TI recommends using external V_{ref} with VREFTX (Ball T17) = V_{DDT} - 0.8 V	
4/5.32900.5	AC Coupled (CFG[13])	0 = AC coupled operation is disabled 1 = AC coupled operation is enabled (Default). AC coupled mode is the only mode supported	
4/5.32900.4	Enable LOL (CFG[12])	0 = Loss of link detection is disabled (Default) 1 = Loss of link detection is enabled	
4/5.32900.3	FASTEQ (CFG[11])	0 = Adaptive equalization set on low data rate 1 = Adaptive equalization set on high data rate (Default)	
4/5.32900.2	ENEQ (CFG[10])	0 = Adaptive equalization is disabled 1 = Adaptive equalization is enabled (Default)	
4/5.32900.1	FASTUPDT (CFG[9])	0 = Fast update mode is disabled (Default) 1 = Fast update mode is enabled	
4/5.32900.0	FASTLOCK (CFG[8])	0 = Fast-lock mode is disabled (Default) 1 = Fast-lock mode is enabled	

(1) Above control bits are only for vendor testing only. Customer should leave them at their default values. They can be accessed from A side or B side.

Table 59. Transmit Pre-emphasis Settings

Mode	CFG[22:19]	100% Swing		62.5% Swing	
		1st Bit	2nd Bit	1st Bit	2nd Bit
Disabled	0000	0%	0%	0%	0%
1 – Tap	0001	5%	0%	9%	0%
	0010	11%	0%	19%	0%
	0011	18%	0%	32%	0%
	0100	25%	0%	47%	0%
	0101	33%	0%	67%	0%
	0110	43%	0%	92%	0%
	0111	67%	0%	178%	0%
	1000	100%	0%	400%	0%

Table 59. Transmit Pre-emphasis Settings (continued)

Mode	CFG[22:19]	100% Swing		62.5% Swing	
		1st Bit	2nd Bit	1st Bit	2nd Bit
2 – Tap	1001	25%	18%	47%	32%
	1010	33%	18%	67%	32%
	1011	33%	25%	67%	47%
	1100	43%	25%	92%	47%
	1101	54%	25%	127%	47%
	1110	82%	54%	257%	127%
	1111	100%	54%	400%	127%

The slew rate of the differential driver may be controlled to suit different transmission media and data rates. This is controlled through CFG [16:15] and CFG [6:5], the effects are shown in the previous table.

Table 60. Slew Rate Control, Tx Rise and Fall Times

CFG[16:15]	CFG[6:5] = 01 or 10		CFG[6:5] = 00	
	MIN	MAX	MIN	MAX
00	90 ps	90 ps	90 ps	104 ps
01	146 ps	146 ps	101 ps	145 ps
10	173 ps	173 ps	126 ps	169 ps
11	281 ps	281 ps	144 ps	196 ps

Table 61. SERDES_CONFIG_2

Address:0x8085		Default:0x0A00	
Bit(s)	Name	Description	Access
4/5.32901.15	JNCSEL (CFG[7])	0 = JOGCOM[0..7] controls whether comma alignment is enabled on lane 0..7 (Default) 1 = JOGCOM[0..7] induces an alignment jog on lane 0..7	RW
4/5.32901.14:13	DATARATE (CFG[6:5])	00 = Full Rate (Default) 01 = Half Rate 10 = Quarter Rate 11 = Reserved	
4/5.32901.12	EN8 (CFG[4])	0 = 10 bit operation (Default) 1 = 8 bit operation	
4/5.32901.11	PLL_LBW (CFG[3])	0 = High loop bandwidth 1 = Low loop bandwidth (Default)	
4/5.32901.10:8	PLLMUL (CFG[2:0])	PLL multiply factor. Can be calculated from following equation. $\text{REFCLK (freq)} = \frac{\text{LINERATE}}{\text{PLLMULTIPLY} \times 2}$ 000 = 5x 001 = 25x 010 = 10x (Default) 011 = 15x 100 = 4x 101 = 20x 110 = 8x 111 = Reserved	

Table 62. SERDES_DATA_CONTROL (1)

Address:0x8086		Default:0xFFFF	
Bit(s)	**Name**	**Description**	**Access**
4/5.32902.15:8	Enable TX	1 = Transmit data pair is enabled for channels 7~0 0 = Transmit data pair is disabled for channels 7~0 (Bit 15 corresponds to channel 7)	RW
4/5.32902.7:0	Enable RX	1 = Receive data pair is enabled for channels 7~0 0 = Receive data pair is disabled for channels 7~0 (Bit 7 corresponds to channel 7)	

(1) When power down mode is enabled using Control register (4/5.0), the SERDES macros go into power down mode where the TX and RX data pairs are disabled for all channels. When A side is powered down, TX and RX data pairs are disabled for channels 3~0. When B side is powered down TX and RX data pairs are disabled for channels 7~4. These low-power modes override the settings in this register. Bits 11:8 corresponds to A side and bits 15:12 corresponds to B side of TX path. Bits 3:0 corresponds to A side and bits 7:4 corresponds to B side of RX path. In normal mode(A side as primary channel, A_B = 1) all the bits needs to be enabled for the normal operation and when B side acts as primary channel(A_B = 0), A side bits can be disabled.

Table 63. SERDES_PLL_CONTROL

Address:0x8087		Default:0x8000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32903.15	PLL Enable	1 = Enabled 0 = Disabled	RW

Table 64. SERDES_SYNC_STATUS

Address:0x8088		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32904.15:8	Sync	Synchronous detect. When high, indicates a comma character has been detected for lanes 7~0 (Feature not supported. Bits made available for future use)	RO
4/5.32904.7:0	Loss of link	Loss of link. When high, indicates that link at the receiver 7~0 lanes is lost (Feature not supported. Bits made available for future use)	

Table 65. SERDES_TESTFAIL_CONTROL

Address:0x8089		Default:0x8000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32905.15	Test fail select	Test fail select controls. According to these selection bits, following Test fail signals will be given out as testfail_mux_out to the Output Pins 0 = TX TESTFAIL selected 1 = RX TESTFAIL selected	RW

Table 66. SERDES_TEST_CONFIG(1)

Address:0x808A			Default:0x0000
Bit(s)	**Name**	**Description**	**Access**
4/5.32906.15:14	TESTCFG[15:14]	Reserved	RW
4/5.32906.13:12	EQTESTMD TESTCFG[13:12]	00 – Equalizer test mode disabled (Default) 01 – 16 Parametric devices observable 10 – 17 Parametric devises are observable 11 – High impedance mode	
4/5.32906.11	PADLPBACK TESTCFG[11]	0 – Pad loop back disabled (Default) 1 – Pad loop back enabled TESTCFG[10] should be enabled else no effect	
4/5.32906.10	LOOPBACK TESTCFG[10]	0 – Loop back disabled (Default) 1 – Loop back enabled (For Internal Test Pattern Verification)	
4/5.32906.9	BSIN	Enable boundary scan inputs. This bit has no affect on transmit SERDES macro.	
4/5.32906.8	BSOUT	Enable boundary scan outputs. This bit has no affect on receive SERDES macro.	
4/5.32906.7:4	AFR TESTCFG[7:4]	Asynchronous frequency ramp mode. Refer **Table 67: Asynchronous frequency ramp mode (Default 4'b0000)**	
4/5.32906.3	TESTCLK TESTCFG[3]	0 – PLL bypass disabled (Default) 1 – PLL bypass enabled	
4/5.32906.2:0	TESTPATT TESTCFG[2:0]	000 – Test pattern gen/verification disabled (Default) 001 – Clock pattern gen/verification enabled 010 – 2^7 - 1 PRBS gen/verification enabled 011 – 2^{23}– 1 PRBS gen/verification enabled 100 – Low frequency clock pattern 101 – Reserved 110 – Reserved 111 – Reserved	

(1) These control bits are only for vendor testing only. Customer should leave them at their default values

Table 67. Asynchronous Frequency Ramp Mode

CFG[9]	AFR	
	TESTCFG[7:4]	**RAMP MODE**
X	XXX0	Disabled
0	0001	- 521 ppm
0	0011	+ 521 ppm
0	0101	- 390 ppm
0	0111	+ 390 ppm
0	1001	- 195 ppm
0	1011	+ 195 ppm
0	1101	- 98 ppm
0	1111	+ 98 ppm
1	0001	- 695 ppm
1	0011	+ 695 ppm
1	0101	- 520 ppm
1	0111	+ 520 ppm
1	1001	- 260 ppm
1	1011	+ 260 ppm
1	1101	- 130 ppm
1	1111	+ 130 ppm

Table 68. REDUNDANCY_CONTROL

Address:0x808B		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32907.4	IDLE	When set, during non retime mode, generates Idle on all lanes of the redundant XAUI channel.	RW
4/5.32907.3	A/B select	When set, channel A is selected as primary else channel B acts as primary channel.	
4/5.32907.2	RETIME	When set, device will go into retime mode else non retime mode. (Default 0)	
4/5.32907.1	XGMII Tristate	When set, puts into a high-impedance state the data outputs on the XGMII side	
4/5.32907.0	Transition code	Output code to be sent during transition from A to B or B to A. When 0 FE, when 1 LF is transmitted.	

Table 69. TRANSITION_TIME_CONTROL

Address:0x808C		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32908.15:0	Transition time	Transition time interval control in 312.5 XGMII clock intervals.	RW

Table 70. REDUNDANCY_COMPOSITE_STATUS

Address:0x808D		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32909.15	IDLE composite	When high, indicates that Idle mode is selected through the REDUNDANCY_CONTROL register on page 56 or through the device input pin.	RO
4/5.32909.14	A_B composite	When high, indicates that lane A is selected as primary lane. It is OR ed version of the REDUNDANCY_CONTROL register bit on page 56 and the device input pin.	
4/5.32909.13	RETIME composite	When high, indicates that device is in RETIME mode. It is OR ed version of the REDUNDANCY_CONTROL register bit on page 56 and the device input pin.	

Table 71. SERDES_JOGCOM_CONTROL (1)

Address:0x808E		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32910.15:8	JOGCOM[7:0]	Jog alignment/ Comma enable bit (one bit per lane). When CFG[7] is set to 0, this bit acts as comma alignment enable control. • JOGCOM[i] = 0 : Comma alignment enabled for lane i • JOGCOM[i] = 1 : Comma alignment disabled for lane i When CFG[7] is set to 1, this bit induces alignment jog on lanes 7..0 • JOGCOM[i] = 0 : Alignment jog disabled for lane i • JOGCOM[i] = 1 : Alignment jog enabled for lane i	RW

(1) These control bits are for vendor testing only. Customer should leave them at their default values

Table 72. DIE_ID_3

Address:0x8090		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32912.15:0	Die ID [63:48]	Bits [63:48] of the Die ID. Unique TI DIE identifier.	RO

Table 73. DIE_ID_2

Address:0x8091			Default:0x0000
Bit(s)	**Name**	**Description**	**Access**
4/5.32913.15:0	Die ID [47:32]	Bits [47:32] of the Die ID. Unique TI DIE identifier.	RO

Table 74. DIE_ID_1

Address:0x8092			Default:0x0000
Bit(s)	**Name**	**Description**	**Access**
4/5.32914.15:0	Die ID [31:16]	Bits [31:16] of the Die ID. Unique TI DIE identifier.	RO

Table 75. DIE_ID_0

Address:0x8093			Default:0x0000
Bit(s)	**Name**	**Description**	**Access**
4/5.32915.15:0	Die ID [15:0]	Bits [15:0] of the Die ID. Unique TI DIE identifier.	RO

Table 76. VTP_MACRO_CONTROL

Address:0x8098			Default:0xBB20
Bit(s)	**Name**	**Description**	**Access**
4/5.32920.15	VTP 1 EN	1 = Enable VTP1 macro (Default) 0 = Disable VTP1 macro Set 0 for Power down or feed through modes	RW
4/5.32920.14	VTP 1 CLK	1 = Enable CLK to change VTP1 macro settings 0 = Disable CLK (Default)	
4/5.32920.13	VTP 1 CLRZ	1 = Initializes VTP1 macro (Default) Enable should be high to reset bits	
4/5.32920.12	VTP 1 LOCK	When set to 1 locks VTP1 bits in their current state. LOCK must be low when setting the VTP1 bits	
4/5.32920.11	VTP 2 EN	1 = Enable VTP2 macro (Default) 0 = Disable VTP2 macro Set 0 for Power down or feed through modes	
4/5.32920.10	VTP 2 CLK	1 = Enable CLK to change VTP2 macro settings 0 = Disable CLK (Default)	
4/5.32920.9	VTP 2 CLRZ	1 = Initializes VTP2 macro (Default) Enable should be high to reset bits	
4/5.32920.8	VTP 2 LOCK	When set to 1 locks VTP2 bits in their current state. LOCK must be low when setting the VTP2 bits	
4/5.32920.7	RESERVED		
4/5.32920.6	Termination Enable	Active LOW termination enable. When 0 enables the termination resistance on the HSTL input.	
4/5.32920.5	Driver Enable	1 = Switching on the HSTL outputs (32 data, 4 control and clock) on the XGMII side is enabled 0 = Switching on the HSTL outputs (32 data, 4 control and clock) on the XGMII side is disabled	

Table 77. VTP1_BIT_CONTROL

Address:0x8099			Default:0xA0C0
Bit(s)	**Name**	**Description**	**Access**
4/5.32921.15	N1IN	N1 signal to be loaded when VTP1 EN = 0	RW
4/5.32921.14	N2IN	N2 signal to be loaded when VTP1 EN = 0	
4/5.32921.13	N3IN	N3 signal to be loaded when VTP1 EN = 0	
4/5.32921.12	N4IN	N4 signal to be loaded when VTP1 EN = 0	
4/5.32921.11	N5IN	N5 signal to be loaded when VTP1 EN = 0	
4/5.32921.10	P1IN	P1 signal to be loaded when VTP1 EN = 0	
4/5.32921.9	P2IN	P2 signal to be loaded when VTP1 EN = 0	
4/5.32921.8	P3IN	P3 signal to be loaded when VTP1 EN = 0	
4/5.32921.7	P4IN	P4 signal to be loaded when VTP1 EN = 0	
4/5.32921.6	P5IN	P5 signal to be loaded when VTP1 EN = 0	

To configure the drive strength values for VTP macros manually, perform the following steps (also see Figure 24) :

1. Disable switching activity on the HSTL outputs by setting VTP_MACRO_CONTROL[5] = LOW.
2. Unlock the macros by writing 0xAA00 to VTP_MACRO_CONTROL register.
3. Enable both macros by writing 0xEE00 followed by 0xAA00 to VTP_MACRO_CONTROL register (this will toggle the CLK for both macros).
4. Clear the macros by writing 0xCC00 followed by 0xAA00 to VTP_MACRO_CONTROL register (this will toggle the CLRZ for both macros).
5. Write the desired pull-down and pull-up strength values to the VTP1_BIT_CONTROL and VTP2_BIT_CONTROL registers for macro 1 and 2 respectively.
6. Write 0xEE00 followed by 0xAA00.
7. Repeat the previous step 64 more times (this toggles the CLK for both macros for 64 cycles). In the first 32 cycles, N1 through N5 bits in the macros are set from bits 11 through 15 of VTP1_BIT_CONTROL and VTP2_BIT_CONTROL registers. In the second 32 cycles, P1 through P5 bits in the macros are set from bits 6 through 10 of VTP1_BIT_CONTROL and VTP2_BIT_CONTROL registers for the corresponding macro.
8. Toggle the CLK for one more cycle (Write 0xEE00 followed by 0xAA00).
9. Write 0xBB20 to lock the macro settings and also enable the switching activity on the outputs.

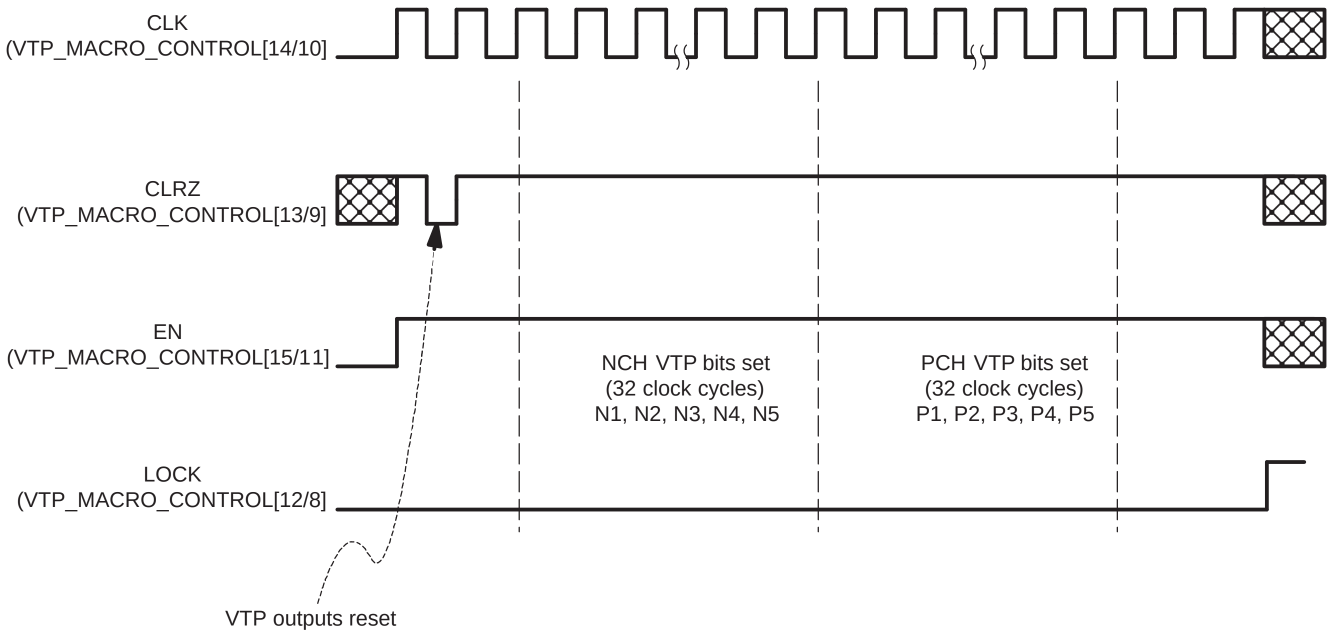


Figure 27. Typical Procedure for Setting Driver Output Impedance

Table 78. VTP2_BIT_CONTROL (1)

Address:0x809A			Default:0xA0C0
Bit(s)	**Name**	**Description**	**Access**
4/5.32922.15	N1IN	N1 signal to be loaded when VTP2 EN = 0	RW
4/5.32922.14	N2IN	N2 signal to be loaded when VTP2 EN = 0	
4/5.32922.13	N3IN	N3 signal to be loaded when VTP2 EN = 0	
4/5.32922.12	N4IN	N4 signal to be loaded when VTP2 EN = 0	
4/5.32922.11	N5IN	N5 signal to be loaded when VTP2 EN = 0	
4/5.32922.10	P1IN	P1 signal to be loaded when VTP2 EN = 0	
4/5.32922.9	P2IN	P2 signal to be loaded when VTP2 EN = 0	
4/5.32922.8	P3IN	P3 signal to be loaded when VTP2 EN = 0	
4/5.32922.7	P4IN	P4 signal to be loaded when VTP2 EN = 0	
4/5.32922.6	P5IN	P5 signal to be loaded when VTP2 EN = 0	

(1) See procedure for setting the drive strength values for the VTP macros in page 61.

OPERATING FREQUENCY RANGE

The TLK3118 is optimized for operation at a serial data rate of 3.125 Gbit/s. The external differential reference clock has an operating frequency of 156.25 MHz. The reference clock frequency must be within ±200 PPM and have less than 40 ps of jitter.

POWERDOWN MODE

The TLK3118 (through both register I/O and pin control) is capable of going into a low power quiescent state. In this state, all analog and digital circuitry is disabled.

DEVICE RESET REQUIREMENTS

Upon application of minimum valid power, the TLK3118 requires reset to be held for at least 10 µs. This allows internal PLLs to stabilize (internal clocks) while internal digital logic is still held in reset. It is also required to provision the HSTL driver controller using the procedure specified in Figure 24.

JITTER TEST PATTERN GENERATION AND VERIFICATION

Use one of the following procedures to generate and verify the respective jitter test pattern:

- **High Frequency Test Pattern**:
  - Issue a hard or soft reset
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register to clear
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register and verify it is cleared. This indicates that the RX link is up.
  - Bypass the Lane Alignment by writing 1 to the RX Lane Align Bypass bit of the RX_BYPASS_CONTROL register.
  - Write “00” to the pattern_select field of the TEST_CONTROL register (4/5.25.1:0).
  - Start the pattern generation on the XAUI_TX and verification on the XAUI_RX by writing “1” to the test_enable bit of the TEST_CONTROL register (4/5.25.2).
  - Read the test pattern error counters for all channels (CHANNEL_0~3_ TEST_ERR_CNT), to clear the counters.
  - At this point the pattern verification is in progress and the errors are reported in the error counters.
  - Reading the counters has no effect on the test except clearing them, i.e. the verification of the pattern continues until the test_enable bit of the TEST_CONTROL register is cleared.
- **Low Frequency Test Pattern**:
  - Issue a hard or soft reset.
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register to clear.
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register and verify it is cleared. This indicates that the RX link is up.
  - Bypass the Lane Alignment by writing 1 to the RX Lane Align Bypass bit of the RX_BYPASS_CONTROL register.
  - Write “01” to the pattern_select field of the TEST_CONTROL register (4/5.25.1:0).
  - Start the pattern generation on the XAUI_TX and verification on the XAUI_RX by writing “1” to the test_enable bit of the TEST_CONTROL register (4/5.25.2).
  - Read the test pattern error counters for all channels (CHANNEL_0~3_ TEST_ERR_CNT), to clear the counters.
  - At this point the pattern verification is in progress and the errors are reported in the error counters.
  - Reading the counters has no effect on the test except clearing them, i.e. the verification of the pattern continues until the test_enable bit of the TEST_CONTROL register is cleared.
- **Mixed Frequency Test Pattern**:
  - Issue a hard or soft reset.
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register to clear.
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register and verify it is cleared. This indicates that the RX link is up.
  - Bypass the Lane Alignment by writing 1 to the RX Lane Align Bypass bit of the RX_BYPASS_CONTROL register.
  - Write “10” to the pattern_select field of the TEST_CONTROL register (4/5.25.1:0).
  - Start the pattern generation on the XAUI_TX and verification on the XAUI_RX by writing “1” to the test_enable bit of the TEST_CONTROL register (4/5.25.2).
  - Read the test pattern error counters for all channels (CHANNEL_0~3_ TEST_ERR_CNT), to clear the counters.
  - At this point the pattern verification is in progress and the errors are reported in the error counters.
  - Reading the counters has no effect on the test except clearing them, i.e. the verification of the pattern continues until the test_enable bit of the TEST_CONTROL register is cleared.
- **Continuous Random Test Pattern (CRPAT)**:
  - Issue a hard or soft reset.
  - Read the test pattern error counter cr_cj_err_cnt registers (4/5.32278 – 4/5.32279) to clear.
  - Write “1” to the crpat_enable bit of the Vendor Specific TEST_CONFIG register (4/5.32768.1).

- Enable the CRPAT verifier by writing 1 to CRPAT Check Enable bit of the TEST_VERIFICATION_CONTROL register (4/5.32769.1).
- In order for the Test Pattern Verifier to start checking the test pattern, it has to receive the Preamble /SFD that is sent at every packet from the test pattern generator. To make sure that the test pattern checking has started, read the 4/5/32801.15 (Test Pattern Status) bit of the Test Pattern Verification Status register. Make sure that the Test Pattern Sync bit is HIGH. If the sync status is not high, this indicates that the verifier never received the Preamble, which may indicate a more severe link problem.
- Perform the test as long as desired.
- Read the CRPAT_CJPAT_TEST_ERROR_COUNT register. Any subsequent counter reads are invalid. If additional reads are required they must be done in separate tests.
- If another test is to be performed go to the first step.

- **Continuous Jitter Test Pattern (CJPAT)**:
  - Issue a hard or soft reset.
  - Read the test pattern error counter cr_cj_err_cnt registers (4/5.32278 – 4/5.32279) to clear.
  - Write “1” to the cjpat_enable bit of the Vendor Specific TEST_CONFIG register (4/5.32768.0).
  - Enable the CJPAT verifier by writing 1 to CJPAT Check Enable bit of the TEST_VERIFICATION_CONTROL register (4/5.32769.0).
  - In order for the Test Pattern Verifier to start checking the test pattern, it has to receive the Preamble /SFD that is sent at every packet from the test pattern generator. To make sure that the test pattern checking has started, read the 4/5/32801.15 (Test Pattern Status) bit of the Test Pattern Verification Status register. Make sure that the Test Pattern Sync bit is HIGH. If the sync status is not high, this indicates that the verifier never received the Preamble, which may indicate a more severe link problem.
  - Perform the test as long as desired.
  - Read the CRPAT_CJPAT_TEST_ERROR_COUNT register. Any subsequent counter reads are invalid. If additional reads are required they must be done in separate tests.
  - If another test is to be performed go to the first step.

If more than one test is specified results are unpredictable.

DEVICE INFORMATION

Table 79. CLOCK PINS

TERMINAL		XGMII NAME	TYPE	DESCRIPTION
NAME	NO.			
REFCLKP/ REFCLKN	R9,R10	N/A	DPECL Input	**Differential Reference Input Clock** This differential pair accepts DPECL compatible signals. AC coupling is required. An on-chip 100-Ω termination resistor is placed differentially between the pins. No external biasing is required. This clock is 156.25 MHz ± 200 ppm
TCLK	F2	TX_CLK	HSTL/ Input	**Transmit Data Clock** This is the input 156.25-MHz ±200 ppm XGMII transmit data path clock input. It is used to sample TXD (31:0), and TXC (3:0).
RCLK	E20	RX_CLK	HSTL/ Output	**Receive Data Clock** This is the output 156.25-MHz ±200 ppm XGMII receive data path clock output. This clock is centered in the middle of the DDR RXD (31:0) and RXC (3:0) data output pins.

Table 80. Serial Side Data Pins

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
TDP30/TDN30 TDP20/TDN20 TDP10/TDN10 TDP00/TDN00	W7,Y7 U8,V8 W9,Y9 U10,V10	CML Output	**Transmit Differential Pairs, XAUI Lane A** High-speed serial outputs. Minimum bit time 320 ps.
TDP31/TDN31 TDP21/TDN21 TDP11/TDN11 TDP01/TDN01	W15,Y15 U16,V16 W17,Y17 U18,V18	CML Output	**Transmit Differential Pairs, XAUI Lane B** High speed serial outputs. Minimum bit time 320 ps.

Table 80. Serial Side Data Pins (continued)

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
RDP30/RDN30 RDP20/RDN20 RDP10/RDN10 RDP00/RDN00	U6,V6 W5,Y5 U4,V4 W3,Y3	CML Input	**Receive Differential Pairs, XAUI Lane A** High-speed serial inputs with on-chip 100-Ω differential termination. Each input pair is terminated differentially across an on chip 100-Ω resistor. Minimum bit time 320 ps. AC coupling required.
RDP31/RDN31 RDP21/RDN21 RDP11/RDN11 RDP01/RDN01	U14,V14 W13,Y13 U12,V12 W11,Y11	CML Input	**Receive Differential Pairs, XAUI Lane B** High speed serial inputs with on-chip 100-Ω differential termination. Each input pair is terminated differentially across an on chip 100-Ω resistor. Minimum bit time 320 ps. AC coupling required.

Table 81. Parallel Data Pins

TERMINAL		XGMII NAME	TYPE	DESCRIPTION
NAME	NO.			
TXD(31:0)	B9, A8, C8, B8, C7, C6, D5, C4, B7 A7, B6, A6 G3, H4, H3 B5, B4, B3 B2, G1, G2 H1, H2, J2 J1, K1, L1 L4, L2, M2 M3, M4	TXD[31:0]	HSTL/ Input	**Transmit Data Pins** Parallel data on this bus is clocked on the rising and falling edge of TCLK.
TXC(3:0)	C9, D3 C2, K4	TXC0	HSTL/ Input	**Transmit Data Control** XGMII Control inputs. This bus is clocked on both edges of TCLK.
RXD(31:0)	C11, D11 D17, D13 D12, C12 B12, C17 C14, C13 B13, B17 D19, D18 E19, C19 H18, C18 B19, F18 F20, G19 G20, H19 K17, H20 K16, J20 L17, K19 K20, L20	RXD(31:0)	HSTL/ Output	**Receive Data Pins** Parallel data on this bus is valid on the rising and falling edge of RCLK. These pins have internal series termination to provide direct connection to a 50-Ω transmission line.
RXC(3:0)	B11, C15 J17, K18	RXC(3:0)	HSTL/ Output	**Receive Data Control** XGMII Control Outputs. This data is valid on both the rising and falling edge of RCLK. These pins have internal series termination to provide direct connection to a 50-Ω transmission line.

Table 82. JTAG Test Port Interface

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
TDI	W19	LVCMOS 2.5V Input (Internal Pullup)	**JTAG Input Data** TDI is used to serially shift test data and test instructions into the device during the operation of the test port.
TDO	V19	LVCMOS 2.5V Output	**JTAG Output Data** TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state.
TMS	U19	LVCMOS 2.5V Input (Internal Pullup)	**JTAG Mode Select** TMS is used to control the state of the internal test-port controller.

Table 82. JTAG Test Port Interface (continued)

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
TCK	Y20	LVCMOS 2.5V Input	**JTAG Clock** TCK is used to clock state information and test data into and out of the device during the operation of the test port.
TRST_N	U20	LVCMOS 2.5V Input (Internal Pullup)	**JTAG Test Reset**– TRST_N is used to reset the JTAG logic into system operational mode.

Table 83. Management Data Interface

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
MDIO	U2	LVCMOS 2.5V I/O	**Management Data I/O** MDIO is the bi-directional serial data path for the transfer of management data to and from the protocol device.
MDC	T2	LVCMOS 2.5V Input	**Management Data Clock** MDC is the clock reference for the transfer of management data to and from the protocol device.
DVAD(4:0)	T1, T3, U1 V1, W1	LVCMOS 2.5V Input	**Management PHY Address** Device Address: DVAD (4:1) is the externally set physical address given to this device used to distinguish one device from another. DVAD (0) is actually used to determine whether the device responds as a DTE (=1) or PHY (=0) XGXS device (4.xxx or 5.xxx on register accesses). These are typically pulled up or pulled down in the system application.

Table 84. Miscellaneous Pins

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
A_B	D7	LVCMOS 2.5V Input	**XAUI Lane Select** In Retime mode, A/B selects which data is reflected on the XGMII outputs. In Redundant Transceiver Modes, A/B selects whether XAUI A or XAUI B data is reflected on the XGMII output interface, if so enabled. A_B = 1 -> A Side Selected A_B = 0 -> B Side Selected
RETIM	N1	LVCMOS 2.5V Input	**Re-Timer Mode Enable** When RETIM is high, serial inputs from XAUI Channels A RX are synchronized and output on XAUI Channels B TX, and vice-versa.
IDLE	N19	LVCMOS 2.5V Input	**IDLE** When RETIME is low, and IDLE is high, IDLE codes (Valid AKR Sequences) will be sent out to the non selected serial interface instead of bridged XGMII transmit traffic packet data. When RETIME is low, and IDLE is low, both XAUI A and XAUI B transmit data will reflect the actual XGMII TX packet data. When RETIME is high, this pin should be considered a don't care input.
RSTN	D9	LVCMOS 2.5V Input	**Chip Reset** When asserted low, this signal reinitializes the entire device. Must be asserted for at least 10 uS after device power up.

Table 85. Voltage Supply and Reference Pins

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
GND	A9, A10, A14, B10, B15, B18, C10, C20, D10, D15, E6, E7, E8, E9, E11, E14, E15, E16, F6, F7, F8, F9, F10, F11, F13, F14, F16, G6, G7, G8, G9, G10, G11, G12, G13, G14, G17, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, J6, J7, J8, J9, J10, J11, J12, J13, J14, J16, J19, K6, K7, K8, K9, K10, K11, K12, K13, K14, L6, L7, L8, L9, L10, L11, L12, L13, L19, M6, M15, N6, N16, N18, P6		Digital Ground.
GNDA	M7, M8, M9, M10, M11, M12, M13, M14, N7, N8, N9, N10, N11, N12, N13, N14, P7, P8, P12, P14, R12, T6, T8, T12, T13, T14, T15, U3, U5, U7, U9, U11, U13, U15, U17, W4, W6, W8, W10, W12, W14, W16, W18		Analog Ground.
VDD	A1, A4, A13, A17, A20, D2, D16, D20, E1, E5, E13, G5, G15, H5, J15, K5, L15, N5, N15, P15, T4, T9, W20		1.2-V Supply (Core Digital Voltage).
VPP	E4		Efuse Controller Voltage (1.2 V) Must be tied to 1.2 V in the system application.
VDDA	R6, P9, P10, P11, P13, R8, R13, R14, R16, T19, V3, V7, V9, V13, V15, Y4, Y6, Y10, Y12, Y16, Y18		1.2-V Analog Supply Voltage.

Table 85. Voltage Supply and Reference Pins (continued)

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
VDDIO	A2, A12, A15, A16, A19, B14, B20, C1, D1, D6, E10, E12, E17, F3, F5, F12, F15, F17, F19, G4 J3, L14, L18, R15, R17, V20, Y1, Y19		2.5-V LVCMOS Input/Output Supply Voltage.
VREF	C5, K2, M17, P17		Input Threshold for HSTL Inputs (0.75 V).
VTT	A3, B1, F1, F4, J5, L5, L16, M16, P16		End Termination Voltage for HSTL Inputs (0.75 V).
VDDQ	E18, G16, G18, H16, J4, K15, M5, P5, R5		HSTL Input/Output Supply Voltage (1.5 V).
VDDT	V5, V11, V17, Y2, Y8, Y14		1.2-V Termination Supply (Used on SERDES Macro).
QGND	D4, L3		Quiet Ground – For HSTL Inputs.
VIATST	W2		Via Test – Grounded In the System Application.
GPI[11:0]	C3, M1, M18, M20, N3, N17, P3, P19, K3, A5, E3, D8	LVCMOS 2.5V Input	General Purpose Input – Must Be Grounded in the System Application.
GPO[23:0]	A11, A18, D14, M19, N2, N4, N20, P1, P2, P4, P18, P20, R1, R2, R3, R7, R11, R18, R20, T7, T11, T18, T20, V2	LVCMOS 2.5V Output	General Purpose Output – Must Be No Connect in the System Application.
NUI	E2		No Connect in the system application.
NUI4	T10		Direct connection to 2.5-V board power plane.
VREFTX	T17		VREF for SERDES TX. (Connect to 1.2 V).
NUI3	R4		No Connect in the system application.
NUI2	T5		No Connect in the system application.
IREFTX	T16		0-Ω connection to 2.5-V power plane.
NUI1	R19		No Connect in the system application.
VTP_PU1	B16		External 50-Ω Pull-Up to VDDQ (1% Tolerance).
VTP_PD1	C16		External 50-Ω Pull-Down to VSS (1% Tolerance).
VTP_PU2	H17		External 50-Ω Pull-Up to VDDQ (1% Tolerance).
VTP_PD2	J18		External 50-Ω Pull-Down to VSS (1% Tolerance).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
Y	VDDIO	VDDT	RDN00	VDDA	RDN20	VDDA	TDN30	VDDT	TDN10	VDDA	RDN01	VDDA	RDN21	VDDT	TDN31	VDDA	TDN11	VDDA	VDDIO	TCLK	Y
W	DVAD0	VIATST	RDP00	GNDA	RDP20	GNDA	TDP30	GNDA	TDP10	GNDA	RDP01	GNDA	RDP21	GNDA	TDP31	GNDA	TDP11	GNDA	TDI	VDD	W
V	DVAD1	NC−GPO	VDDA	RDN10	VDDT	RDN30	VDDA	TDN20	VDDA	TDN00	VDDT	RDN11	VDDA	RDN31	VDDA	TDN21	VDDT	TDN01	TDO	VDDIO	V
U	DVAD2	MDIO	GNDA	RDP10	GNDA	RDP30	GNDA	TDP20	GNDA	TDP00	GNDA	RDP11	GNDA	RDP31	GNDA	TDP21	GNDA	TDP01	TMS	TRSTN	U
T	DVAD4	MDC	DVAD3	VDD	NUI2	GNDA	NC−GPO	GNDA	VDD	NUI4	NC−GPO	GNDA	GNDA	GNDA	GNDA	IREFTX	VREFTX	NC−GPO	VDDA	NC−GPO	T
R	NC−GPO	NC−GPO	NC−GPO	NUI3	VDDQ	VDDA	NC−GPO	VDDA	REFCLKP	REFCLKN	NC−GPO	GNDA	VDDA	VDDA	VDDIO	VDDA	VDDIO	NC−GPO	NUI1	NC−GPO	R
P	NC−GPO	NC−GPO	GND−GPI	NC−GPO	VDDQ	GND	GNDA	GNDA	VDDA	VDDA	VDDA	GNDA	VDDA	GNDA	VDD	VTT	VREF	NC−GPO	GND−GPI	NC−GPO	P
N	RETIME	NC−GPO	GND−GPI	NC−GPO	VDD	GND	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	VDD	GND	GND−GPI	GND	IDLE	NC−GPO	N
M	GND−GPI	TXD2	TXD1	TXD0	VDDQ	GND	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GND	VTT	VREF	GND−GPI	NC−GPO	GND−GPI	M
L	TXD5	TXD3	QGND	TXD4	VTT	GND	GND	GND	GND	GND	GND	GND	GND	VDDIO	VDD	VTT	RXD3	VDDIO	GND	RXD0	L
K	TXD6	VREF	GND−GPI	TXC0	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDQ	RXD5	RXD7	RXC0	RXD2	RXD1	K
J	TXD7	TXD8	VDDIO	VDDQ	VTT	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	GND	RXC1	VTP_PD2	GND	RXD4	J
H	TXD10	TXD9	TXD17	TXD18	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDDQ	VTP_PU2	RXD15	RXD8	RXD6	H
G	TXD12	TXD11	TXD19	VDDIO	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDDQ	GND	VDDQ	RXD10	RXD9	G
F	VTT	TCLK	VDDIO	VTT	VDDIO	GND	GND	GND	GND	GND	GND	VDDIO	GND	GND	VDDIO	GND	VDDIO	RXD12	VDDIO	RXD11	F
E	VDD	NUI	GND−GPI	VPP	VDD	GND	GND	GND	GND	VDDIO	GND	VDDIO	VDD	GND	GND	GND	VDDIO	VDDQ	RXD17	RCLK	E
D	VDDIO	VDD	TXC2	QGND	TXD25	VDDIO	A_B	GND−GPI	RSTN	GND	RXD30	RXD27	RXD28	NC−GPO	GND	VDD	RXD29	RXD18	RXD19	VDD	D
C	VDDIO	TXC1	GND−GP1	TXD24	VREF	TXD26	TXD27	TXD29	TXC3	GND	RXD31	RXD26	RXD22	RXD23	RXC2	VTP−PD1	RXD24	RXD14	RXD16	GND	C
B	VTT	TXD13	TXD14	TXD15	TXD16	TXD21	TXD23	TXD28	TXD31	GND	RXC3	RXD25	RXD21	VDDIO	GND	VTP−PU1	RXD20	GND	RXD13	VDDIO	B
A	VDD	VDDIO	VTT	VDD	GND−GP1	TXD20	TXD22	TXD30	GND	GND	NC−GPO	VDDIO	VDD	GND	VDDIO	VDDIO	VDD	NC−GPO	VDDIO	VDD	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 28. Pin Out (Bottom View)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

	UNIT
Supply voltage[2], V_{DD}, V_{DDA}	-0.3 V to 1.5 V
Supply voltage[2], V_{DDQ}	-0.3 V to 2.5 V
Supply voltage[2], V_{DDB}	-0.3 V to 3 V
Supply voltage[2], V_{DDT}	-0.3 V to 2 V
Input Voltage, V_I (LVCMOS)	-0.5 V to 3 V
Input Voltage, V_I (HSTL CLASS 1)	-0.5 V to 2 V
Electrostatic Discharge	HBM: 2 kV, CDM: 750 V
Storage temperature, T_{stg}	-65°C to 150°C
Operating free-air temperature range, T_A	0°C to 70°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}, Core supply voltage		1.14	1.2	1.26	V
V_{DDB}, Bias supply voltage	LVCMOS I/O	2.37	2.5	2.63	V
V_{DDT}, Bias supply voltage		1.14	1.2	1.26	V
V_{DDQ}, I/O supply voltage	HSTL Class 1	1.4	1.5	1.6	V
V_{DDA}, Analog supply voltage		1.14	1.2	1.26	V
I_{DD}, Core supply current	R_{ω} = 156.25 MHz			770	mA
I_{DDQ}, I/O supply current	R_{ω} = 156.25 MHz			415	mA
I_{DDB}, Bias supply current	R_{ω} = 156.25 MHz			35	mA
I_{DDA}, Analog supply current	R_{ω} = 156.25 MHz			240	mA
P_D, Total power consumption	R_{ω} = 156.25 MHz		2.09	2.4	W
V_{REF}, Input reference voltage[1]	HSTL Class 1	0.71	0.75	0.79	V
I_{SDA}, Analog shutdown current			0.5		mA
I_{SDD}, Core shutdown current			11		mA

(1) The value of V_{REF} may be selected to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}. Peak-to-peak ac noise on V_{REF} may not exceed ± 2% VREF (dc).

REFERENCE CLOCK TIMING REQUIREMENTS (REFCLKP/N)[1]

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	Minimum data rate	TYP-0.01%	125	TYP+0.01%	MHz
	Maximum data rate	TYP-0.01%	156.25	TYP+0.01%	
Accuracy		-200		200	ppm
Duty cycle		40%	50%	60%	
Jitter	Random and deterministic			40	ps

(1) This clock should be crystal referenced to meet the requirements of the above table. Contact your local TI sales office for specific clocking recommendations.

REFERENCE CLOCK ELECTRICAL CHARACTERISTICS (REFCLKP/N)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	Differential input voltage		250		2000	mVp-p
C_I	Input capacitance				3	pF
R_I	Differential input impedance		80	100	120	Ω

LVCMOS ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -100 µA, Driver Enabled	V_{DDO}-0.2			V
V_{OL}	Low-level output voltage	I_{OH} = -100 µA, Driver Enabled			0.2	V
V_{IH}	High-level input voltage		0.7×V_{DDO}			V
V_{IL}	Low-level input voltage		0		0.3×V_{DDO}	V
I_{IH},I_{IL}	High-level/low-level input current				±1	µA
I_{IZ}	Low-impedance input current	Driver Only, driver disabled			±20	µA
C_I	Input capacitance				5	pF
V_{pad}	Voltage at PAD				V_{DDO}	

HSTL SIGNALS ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(dc)}$	High-level output voltage		V_{DDO}-0.4		V_{DDO}	V
$V_{OL(dc)}$	Low-level output voltage				0.4	V
$V_{OH(ac)}$	High-level output voltage		V_{DDO}-0.5		V_{DDO}	V
$V_{OL(ac)}$	Low-level output voltage				0.5	V
$V_{IH(dc)}$	High-level input voltage, DC	DC input, logic high	V_{REF}+0.1		V_{DDO}+0.3	V
$V_{IL(dc)}$	Low-level input voltage, DC	DC input, logic low	-0.3		V_{REF}-0.1	V
$V_{IH(ac)}$	High-level input voltage, AC	AC input, logic high	V_{REF}+0.2			V
$V_{IL(ac)}$	Low-level input voltage, AC	AC input, logic low			V_{REF}-0.2	V
$I_{OH(dc)}$	High-level output current	V_{DDQ} = 1.5 V	-8			mA
$I_{OL(dc)}$	Low-level output current	V_{DDQ} = 1.5 V	8			mA
C_I	Input capacitance				4	pF

HSTL INPUT TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{su}	Setup time, TXD[31:0], TXC[3:0] setup prior to TCLK transition high or low	Timing relative to V_{REF}	-368	-197	-39	ps
t_h	Hold time, TXD[31:0], TXC[3:0] Hold after TCLK transition high or low	Timing relative to V_{REF}	-442	-211	-130	ps

SERIAL TRANSMITTER/RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(pp)}$	TX output differential peak-to-peak voltage swing	Maximum pre-emphasis enabled. See Figure 29.(emphasized bit)	730	860	970	mVp-p
$V_{OD(pd)}$		Pre-emphasis enabled. See Figure 29. (de-emphasized bit)	440	526	600	mVp-p
		Max pre-emphasis disabled	840	1010	1100	mVp-p
I_{IKG}	RX input leakage current		-10		10	µA
C_I	Input capacitance				2	pF

SERIAL TRANSMITTER/RECEIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r, t_f	Differential output signal rise, fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, See Figure 29.	80		160	ps
J_{TOL}	Jitter tolerance, total jitter at serial input	Zero crossing, See Figure 32.			0.6	UI (1)
J_{DR}	Serial input deterministic jitter	Zero crossing, See Figure 32.			0.36	UI (1)
J_T	Serial output total jitter	PRBS @ 3.125 GHz.		0.2	0.35	UI (1)
J_D	Serial output deterministic jitter	PRBS @ 3.125 GHz.			0.17	UI (1)
t_d	Total delay from RX input to RD output	See Figure 9.			700	Bit Times
t_d	Total delay from TD input to TX output	See Figure 8.			600	Bit Times

(1) Unit Interval = one serial bit time (min. 320ps)

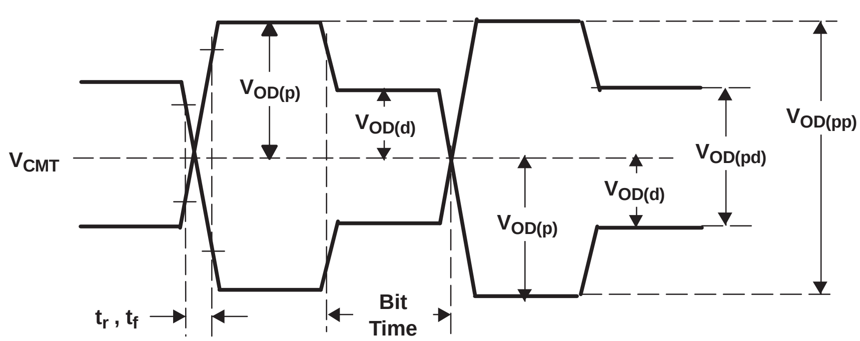
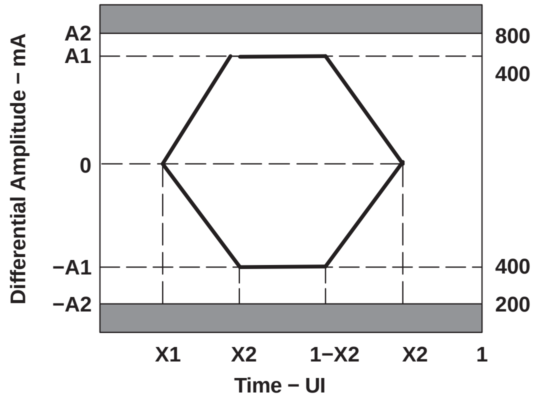


Figure 29. Transmit Output Waveform Parameter Definitions



$$\left(VREFTX = V_{DDT} - 0.8\ V\right)$$

Figure 30. Transmit Template

Table 86. Driver Template Parameters(1)

PARAMETER	NEAR END VALUE	FAR END VALUE	UNIT
X1 (See Figure 30, Transmit Template)	0.175	0.275	UI
X2 (See Figure 30, Transmit Template)	0.390	0.400	UI
A1 (See Figure 30, Transmit Template)	400	100	mV
A2 (See Figure 30, Transmit Template)	800	800	mV

(1) For xAUI compliance use external V_{ref}.

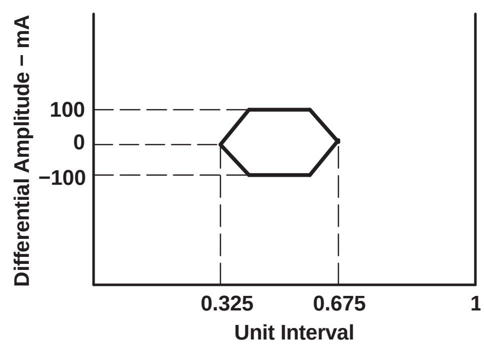
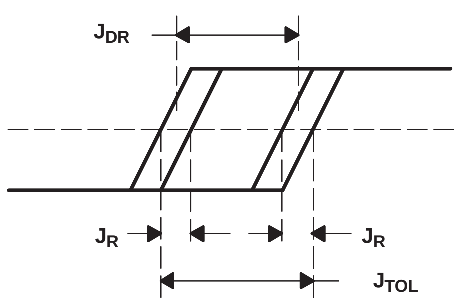


Figure 31. Receive Template



NOTE: $J_{TOL} = J_R + J_{DR}$, where J_{TOL} is the receive jitter tolerance, J_{DR} is the received deterministic jitter, and J_R is the Gaussian random edge jitter distribution at a maximum BER = 10^{-12}.

Figure 32. Input Jitter

HSTL OUTPUT SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{su}	Setup time, RXD[31:0], RXC[3:0] setup prior to RCLK transition high or low	See Figure 33.	960			ps
t_h	Hold time, RXD[31:0], RXC[3:0] hold after RCLK transition high or low	See Figure 33.	960			ps
DC	Duty cycle, RCLK		45%		55%	

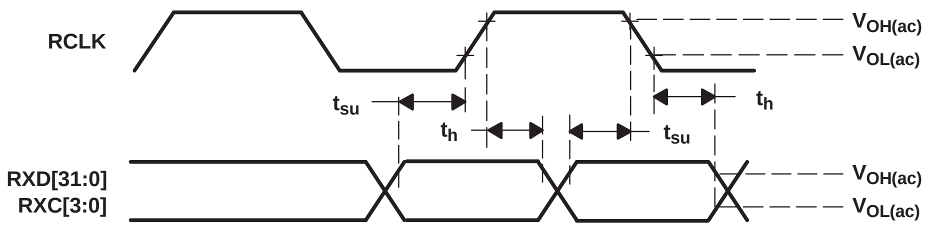


Figure 33. HSTL Output Timing Diagram

HSTL INPUT TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{su}	Setup time, TXD [31:0], TXC[3:0] setup prior to TCLK transition high or low	See Figure 34.	480			ps
t_h	Hold time, TXD[31:0], TXC[3:0] hold after TCLK transition high or low	See Figure 34.	480			ps
DC	Duty cycle, TCLK		45%		55%	

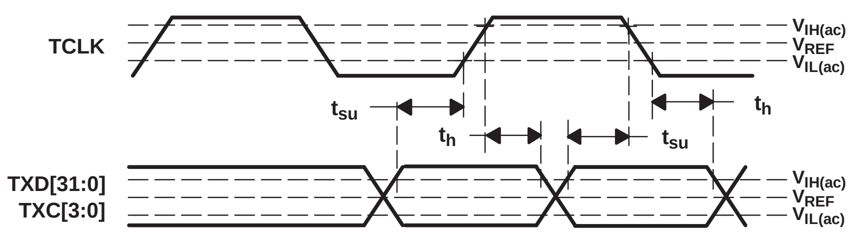


Figure 34. HSTL Data Input Timing Diagram

MDIO TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{period}	MDC period	See Figure 35.	400			ns
t_{su}	MDIO setup to ↑ MDC	See Figure 35.	10			ns
t_h	MDIO hold to ↑ MDC	See Figure 35.	10			ns

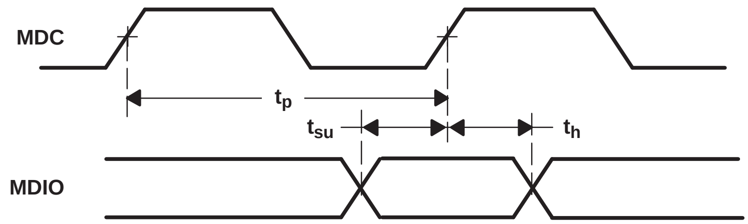


Figure 35. MDIO Read/Write Timing Diagram

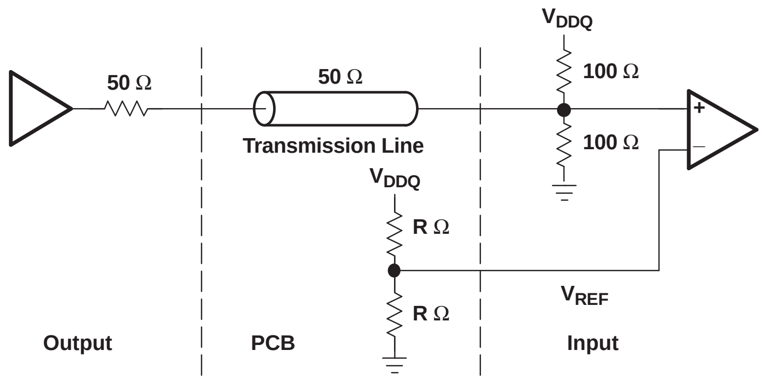


Figure 36. HSTL I/O

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Page numbers for previous versions may differ from page numbers in the current version.

Changes from B Revision (August, 2006) to C Revision	Page
• Changed Moved "Start the pattern generation" prior to "Read the test pattern" (3 locations)	43

Changes from A Revision (April, 2005) to B Revision	Page
• Changed Format (Superscripted values)	1
• Changed to "The reciever input is internally biased to 2xVDDT/3 which is the optimum voltage for input sensitivity" from "Register bit 4/5.32900.5 is used to switch between AC and DC coupled at the receiver. When AC couple is selected, the receiver input is internally biased to 2xVDDT/3 which is the optimum voltage for input sensitivity."	19
• Deleted "Register bit 4/5.32900.5 is used to switch between AC and DC coupled at the receiver. When the receiver is AC coupled, "	20
• Changed to "AC coupling is always required on receiver inputs." from "When the receiver is DC coupled, the common mode will be determined by both receiver and transmitter characteristics."	20
• Changed "4" to "5"	22
• Changed "5" to "4"	22
• Clarified text in the figure	23
• Changed to "VREFTX (Ball T17)" from "Vref"	35
• Added "AC coupled mode is the only mode supported"	35
• Added "AC coupling required"	45
• Added "AC coupling required"	45
• Deleted "Vcmr" characteristics	52
• Added "(VREFTX = VDDT - 0.8V)" to figure	53
• Deleted "(Vref = VDDT - 0.8V)" from figure	53
• Added "400" to MIN column	54
• Deleted "500" from MAX column	54

Changes from Original (December, 2004) to A Revision	Page
• Changed MIN and MAX setup times for HSTL input timing requirements	51
• Changed MIN and MAX hold times for HSTL input timing requirements	51

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLK3118GDV	ACTIVE	FCBGA	GDV	400	60	TBD	SNPB	Level-4-220C-72 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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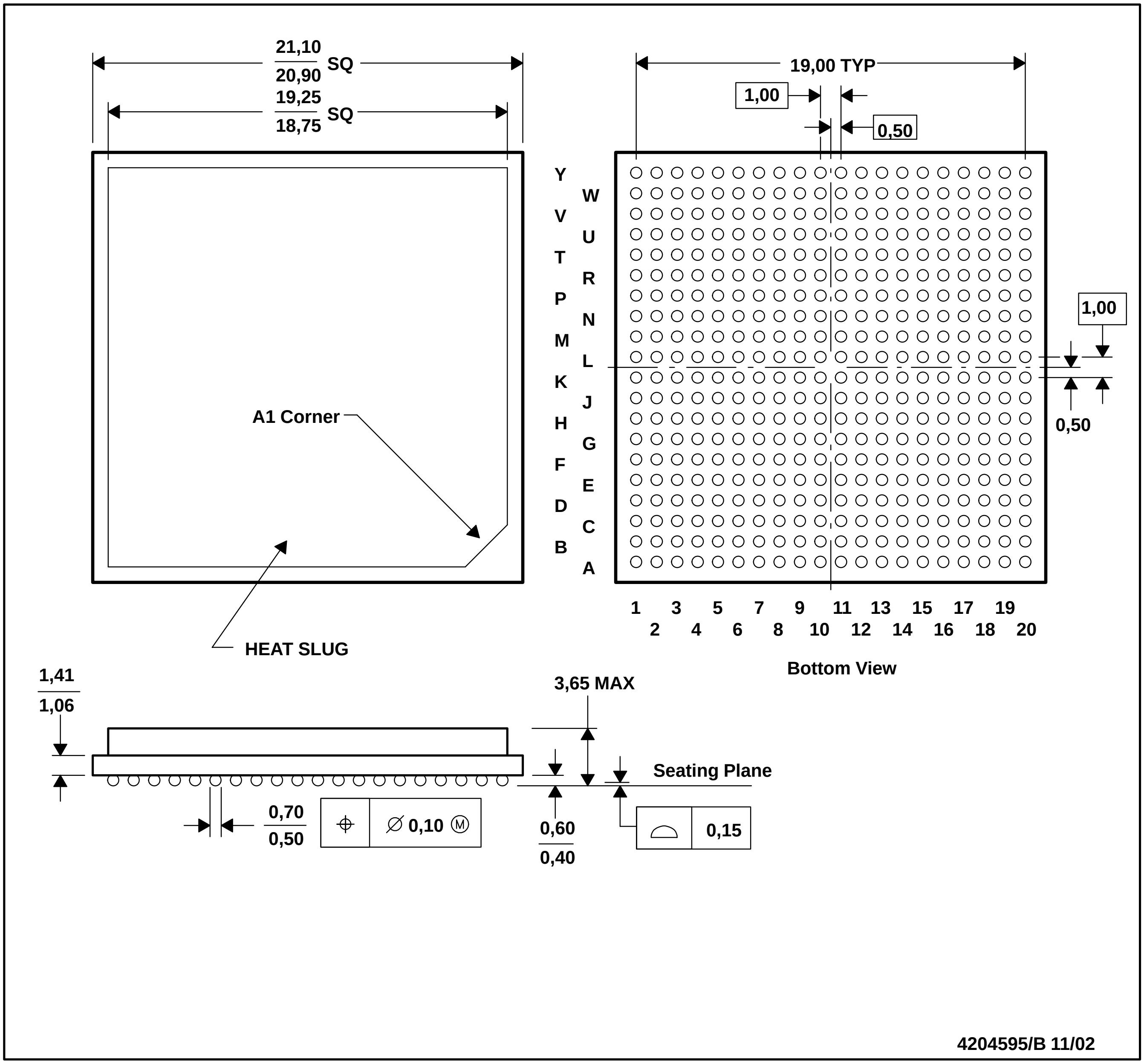
GDV (S-PBGA-N400) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced plastic package with heat slug (HSL).
D. Flip chip application only.

IMPORTANT NOTICE